

LCFC Confidential

BL460


(L460)

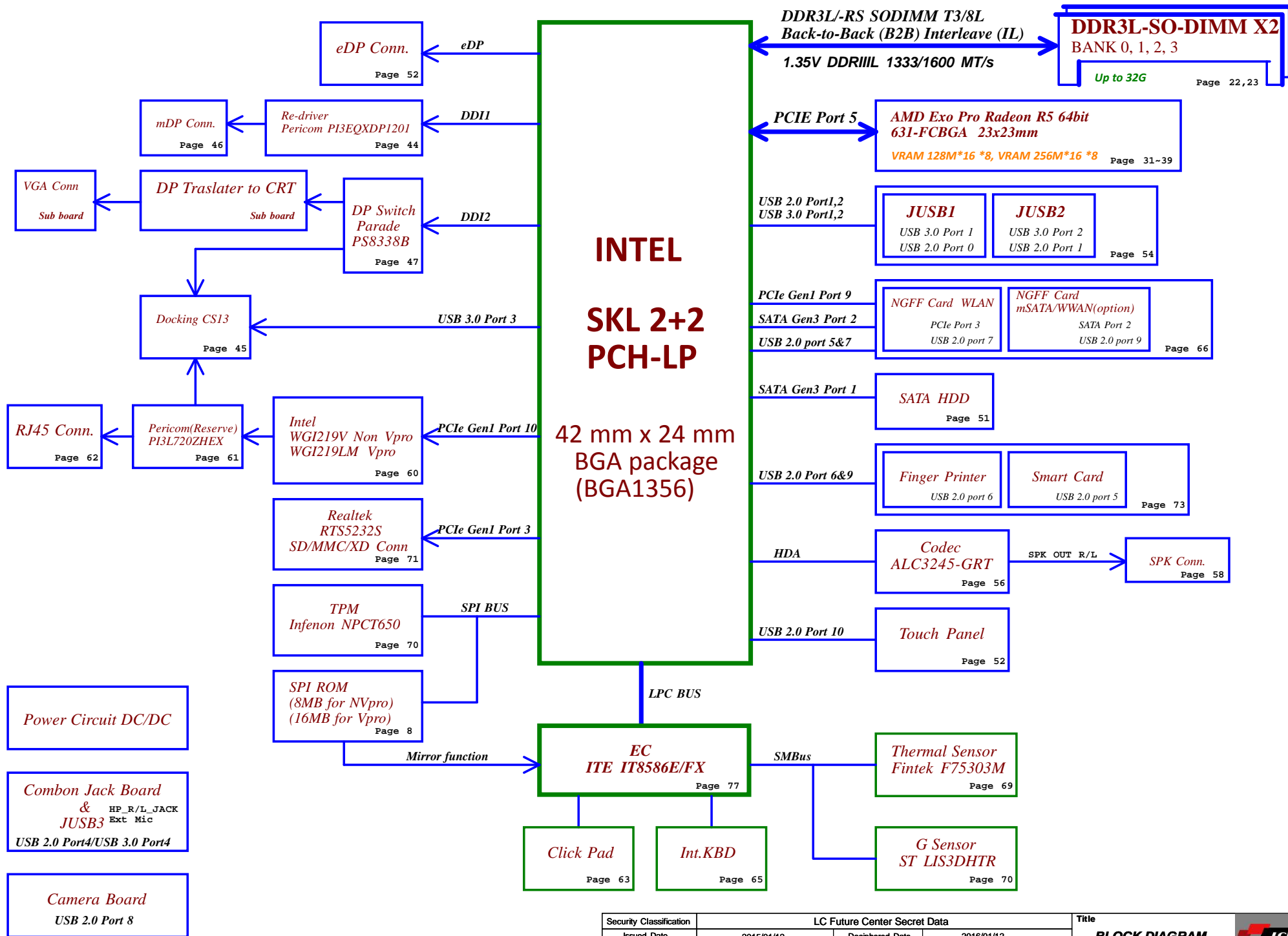
NM-A651 Rev1.0 Schematic

Intel SKL Processor with DDRIII L + PCH

AMD Exo Pro Radeon R5 64bit

2015-10-22 Rev1.0

Security Classification	LC Future Center Secret Data			Title		
Issued Date	2015/01/12	Deciphered Date	2016/01/12	COVER PAGE		
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				Custom	<i>BL460 NM-A651</i>	0.1
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Voltage Rails

O --> Means ON
X --> Means OFF

Power Plane / State	B+	+1VALW +3VALW +1.8VALW +5VALW	+1.35V +0.675VS +VCC_ST	+5VS +3VS +VCC_CORE +VCC_GT +VCC_SA +VCC_IO +VCC_STG +VGA_CORE +1.5VS +0.95VS_VGA +1.5VS_VGA +1.8VS_VGA +3VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

	SIGNAL						
STATE	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	VM_PWRON	EC_ON	SUSP#
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	ON	OFF

SMBUS Control Table

	SOURCE	Main VGA	BATT	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	CP Module	Security ROM	LAN PHY
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL	X	V +3VALW	X	X	X	X	X	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3V_PCH	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3V_PCH	X	X	V +3VS	V +3VS	V +3VS	X	V +5VS	V +3VS	X
PCH_SML0_CLK PCH_SML0_DAT	PCH +3V_PCH	X	X	X	X	X	X	X	X	V +3VALW

HSIO Port

Port	Device
1	USB3.0 port (On Board)
2	USB3.0 port (On Board)
3	USB3.0 port (Docking)
4	USB3.0 port (Sub Board)
5	N/A
6	N/A
7	PCIE (Card Reader)
8	N/A
9	PCIE (GPU)
10	PCIE (GPU)
11	PCIE (GPU)
12	PCIE (GPU)
13	PCIE (WLAN)
14	PCIE (LAN)
15	SATA (HDD)
16	SATA (NGFF)

USB2.0 Port

Port	Device
1	USB port (On Board)
2	USB port (On bBoard)
3	USB port (Docking)
4	USB port (Sub Board)
5	WWAN
6	Finger Printer
7	BT
8	Camera
9	Smart Card
10	Touch Panel

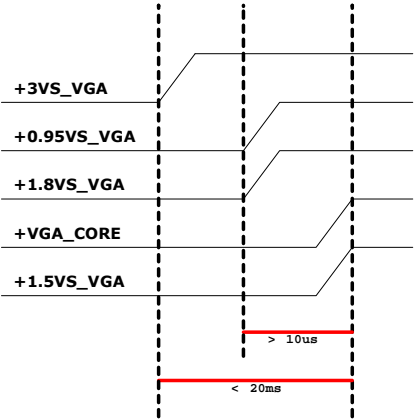
VGA GPIO (EXO-PRO-S3)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	N/A	
GPIO5	IN		GPIO5_AC_BATT
GPIO6	IN		GPIO6
GPIO7	OUT	N/A	
GPIO8	OUT	N/A	GPIO8_ROMSO
GPIO9	OUT	N/A	GPIO9_ROMSI
GPIO10	OUT	N/A	GPIO10_ROMSCK
GPIO11	OUT	N/A	
GPIO12	OUT	N/A	
GPIO13	OUT	N/A	
GPIO15	IN		SVI2_SVD
GPIO16	OUT	N/A	
GPIO17	OUT	N/A	
GPIO19	OUT	N/A	GPIO19_CTF
GPIO20	IN		SVI2_SVC
GPIO21	OUT	N/A	
GPIO22	OUT	N/A	GPIO22_ROMCSB
GPIO29	OUT	N/A	
GPIO30	OUT	N/A	

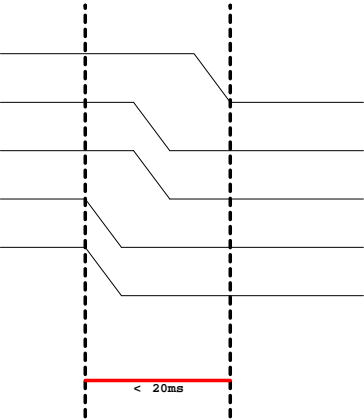
BOM Structure Table

BOM Structure	NOTE
PCB@	For PCB load BOM
3G@	3G function with WWAN
DIS@	Discreate SKU
UMA@	UMA SKU
DPRE@	With DP re-driver
NODPRE@	Bypass DP re-driver
NVPRO@	For Non-VPRO function
VPRO@	For VPRO function
MIRROR@	For mirror function
TPM@	TPM function
X76@	GPU VRAM Setting
XDP@	XDP function
EXO@	EXO function
ME@	ME Connector
EMC@	For EMC function
EMC_NS@	For EMC function (no mount)
RF@	For RF function
RF_NS@	For RF function (no mount)

GPU POWER UP sequence

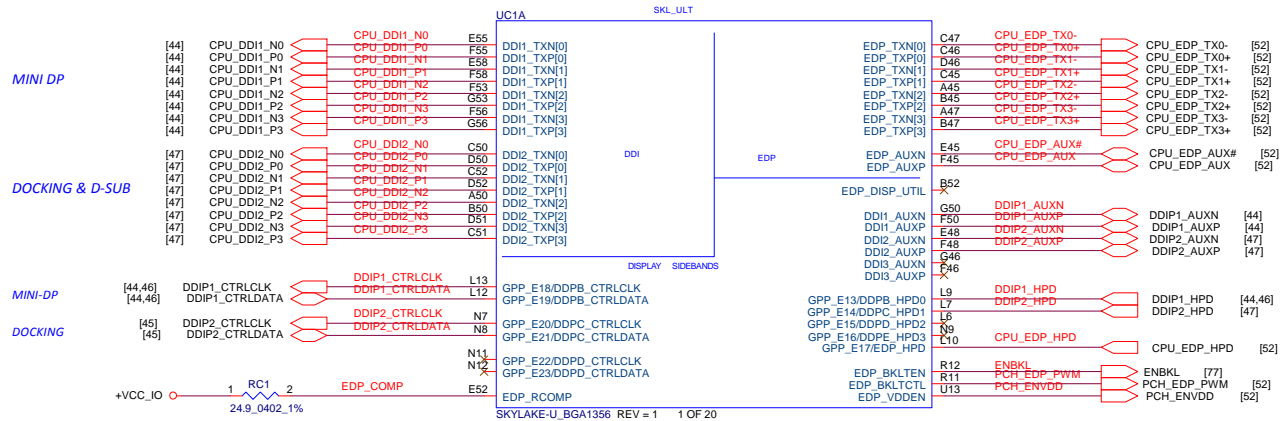


GPU POWER DOWN sequence

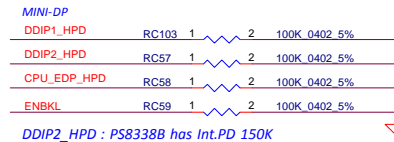
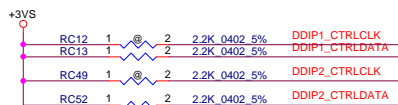


	Device ID
EXO-pro	6660

GPU		EXO-Pro-S3	
VRAM (GDDR3)		PS_3 (RV104)	PS_3 (RV105)
Samsung 1000MHz			
	K4W4G1646E-BC1A (2G)	PH 3.4K	PD 10K
Hynix 1000MHz			
	H5TC4G63CFR-N0C (2G)	PH 4.75K	NC
Micro 1000MHz			
	MT41J256M16HA-093G:E (2G)	PH 3.24K	PD 5.62K

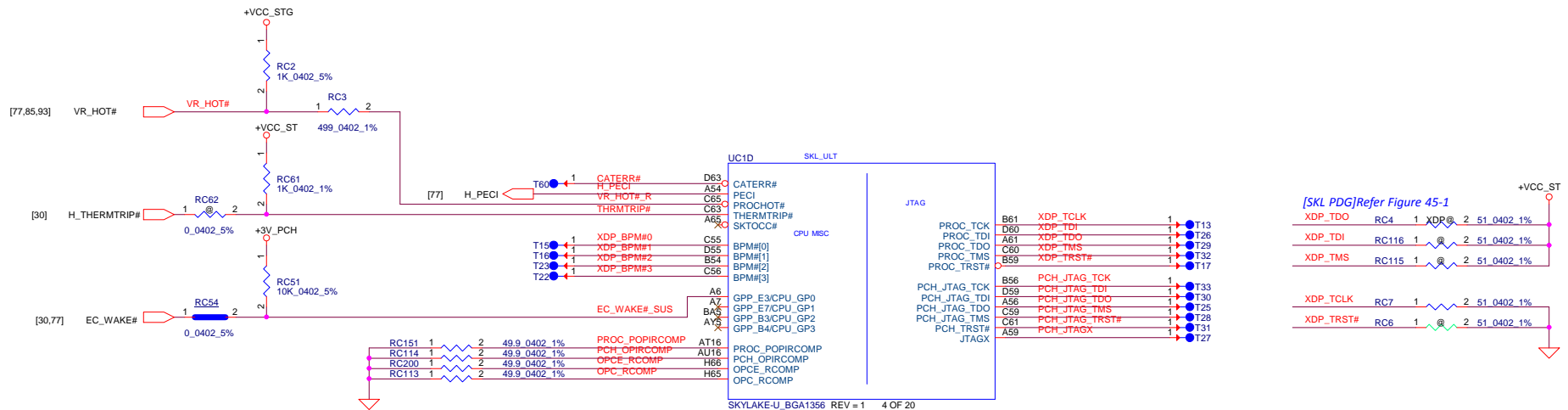


EDP_RCOMP
 1. Trace width=20 mils, Spacing=25mil, Max length=100mils
 2. RC1 close to MCP
 Trace Width=20mil, Spacing=25mil, Max length=100mil

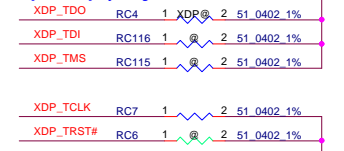


DP port	Enable	Disable
DDPB_CTRLDATA	pull-high	no connect
DDPC_CTRLDATA	pull-high	no connect





[SKL PDG]Refer Figure 45-1





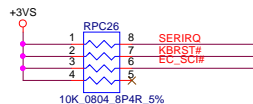
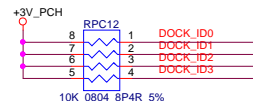
Security Classification		LC Future Center Secret Data		Title		
Issued Date	2015/01/12	Deciphered Date	2016/01/12	SKL_XDP/JTAG		
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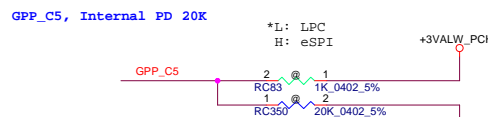
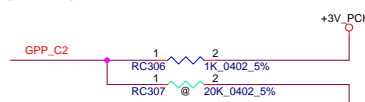
Diagram illustrating the SPI interface between the SD3000 and the RP32 microcontroller. The RP32 is connected to the SD3000 via an 8-pin SPI interface. The connections are as follows:

RP32 Pin	SD3000 Pin	Signal Name
1	1	SPL_I03_8MB
2	2	SPL_CLK_8MB
3	3	SPL_SI_8MB
4	4	SPL_IO2_8MB
5	5	SPL_I03
6	6	SPL_CLK
7	7	SPL_SI
8	8	SPL_IO2

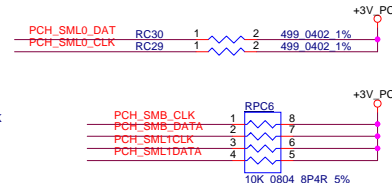
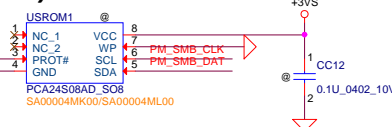
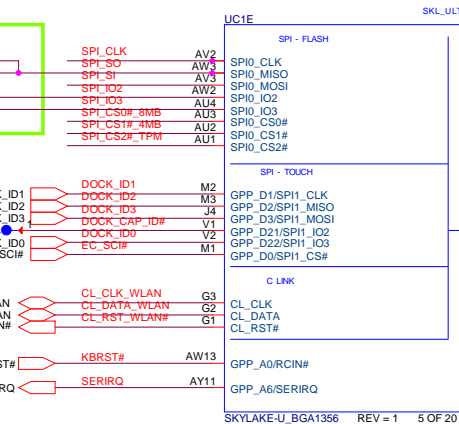
The SD3000 is labeled with the part number 33_0B04_8P4R_5% and the manufacturer code SD30000370T.



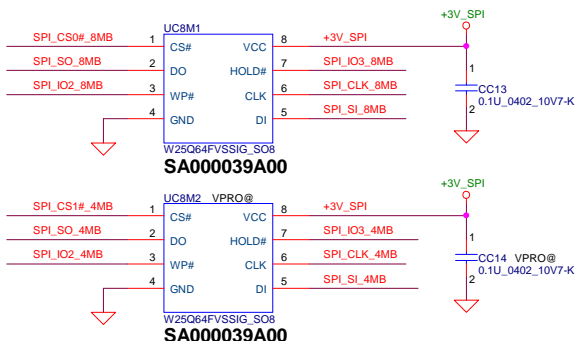
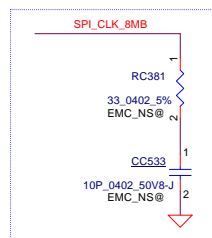
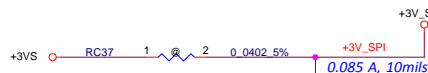
```
L:Disable Intel ME Crypto TLS cipher suite (no confidentiality).
*H:Enable Intel ME Crypto Transport Layer Security (TLS) cipher
suite (with confidentiality).Support Intel AMT with TLS and Intel
SBA (Small Business Advantage) with TLS.
GPP C2, Internal PD 20K
```



[70] SPI_CLK SPI_CLK
 [70] SPI_SI SPI_SI
 [70] SPI_SO SPI_SO
 [70] SPI_CS2#_TPM SPI_CS2#_TPM



+3VM = +3V_{SPI}
 1. VPRO : Q6, +3VLAW To +3VM
 2. NVPRO :
 a. R17 and RC38, +3VALW to +3VM



The schematic diagram illustrates the PMBus interface for three chips: OC1A, OC1B, and OC2A. The chips are connected to the PCH_SMB_CLK and PCH_SMB_DATA lines, which are then connected to the PM_SMB_CLK and PM_SMB_DAT lines. The OC1A and OC1B chips are also connected to the PCH_SML1CLK and PCH_SML1DATA lines, which are then connected to the EC_SMB_CK3 and EC_SMB_DA3 lines. The OC2A chip is connected to the PCH_SML1CLK and PCH_SML1DATA lines, which are then connected to the EC_SMB_CK3 and EC_SMB_DA3 lines. The diagram also shows a +3VS supply and a resistor RC36 (4.7K, 0402, 5%).

Chip Details:

- OC1A: 2N7002KDW, SOT363-6, SB000013A00
- OC1B: 2N7002KDW, SOT363-6, SB000013A00
- OC2A: 2N7002KDW, SOT363-6, SB000013A00

Resistor Details:

- RC36: 4.7K, 0402, 5%

Connections:

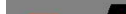
- PCH_SMB_CLK to PM_SMB_CLK
- PCH_SMB_DATA to PM_SMB_DAT
- PCH_SML1CLK to EC_SMB_CK3
- PCH_SML1DATA to EC_SMB_DA3

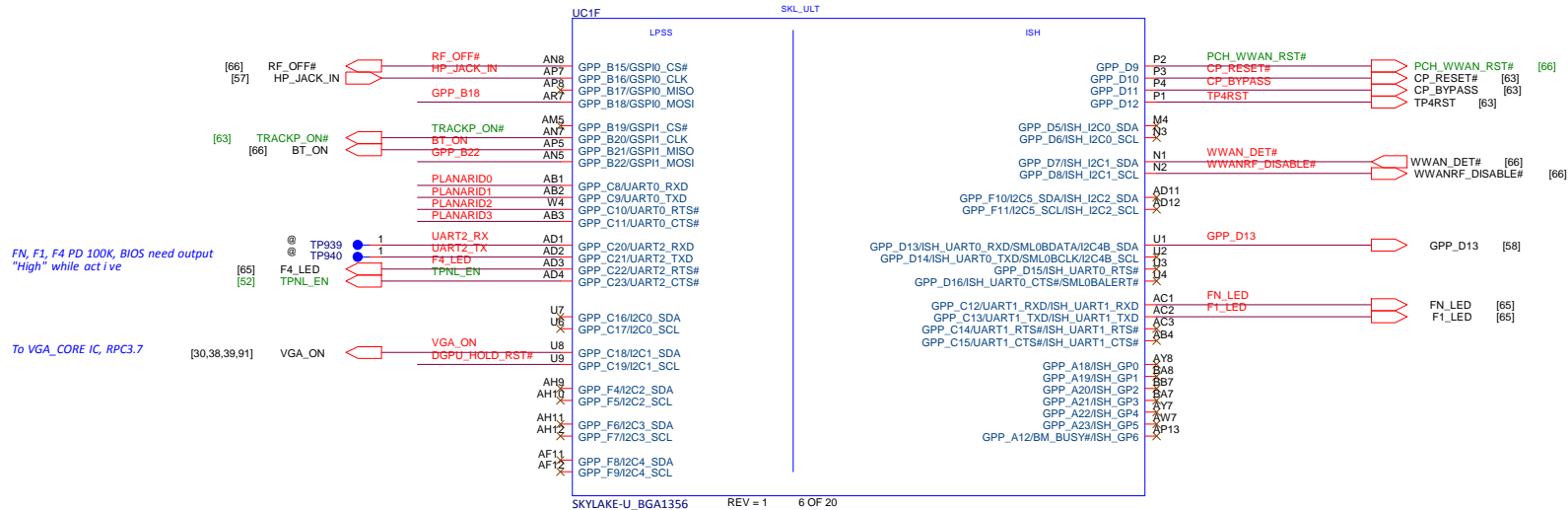
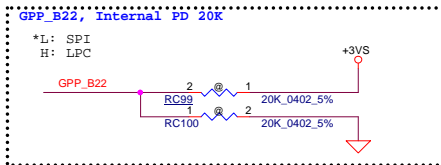
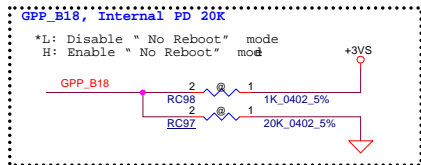
Additional Labels:

- GPU, Thermal Sensor, Embedded Controller, G sensor

FSCE#	SPI_FMOSI#	RE1	1	2	0	0402	5%	SPI_CS0#_8MB
[77]	SPI_FMOSI#	RE2	1	2	0	0402	5%	SPI_ST_8MB
[77]	SPI_FMISO#	RE3	1	2	0	0402	5%	SPI_SO_8MB
[77]	SPI_FMISO	RE4	1	2	0	0402	5%	SPI_CLK_8MB
[77]	SPI_FSCCK							

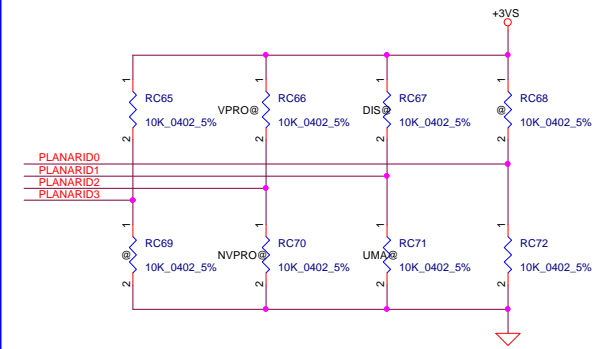
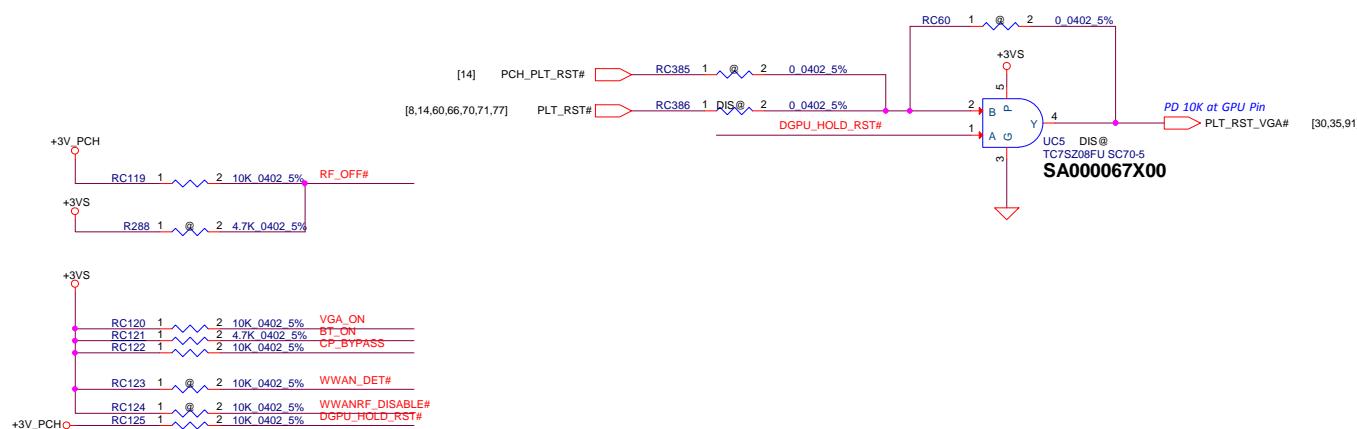
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SKL_LPC/SPI/SMBUS			
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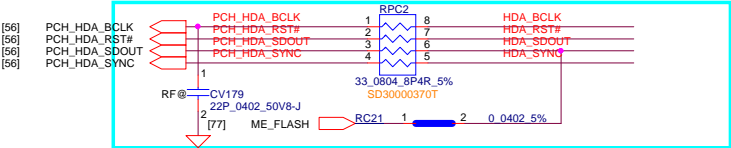


Project/SKU ID

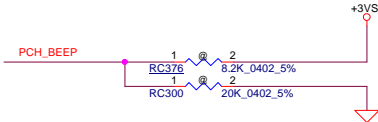
	PLANARID3 (GPP_C11)	PLANARID2 (GPP_C10)	PLANARID1 (GPP_C9)	PLANARID0 (GPP_C8)
1	1(RC65)	VPRO SKU (RC66)	DIS (RC67)	15" (RC68)
0	X	NVPRO SKU (RC70)	UMA (RC71)	14" (RC72)



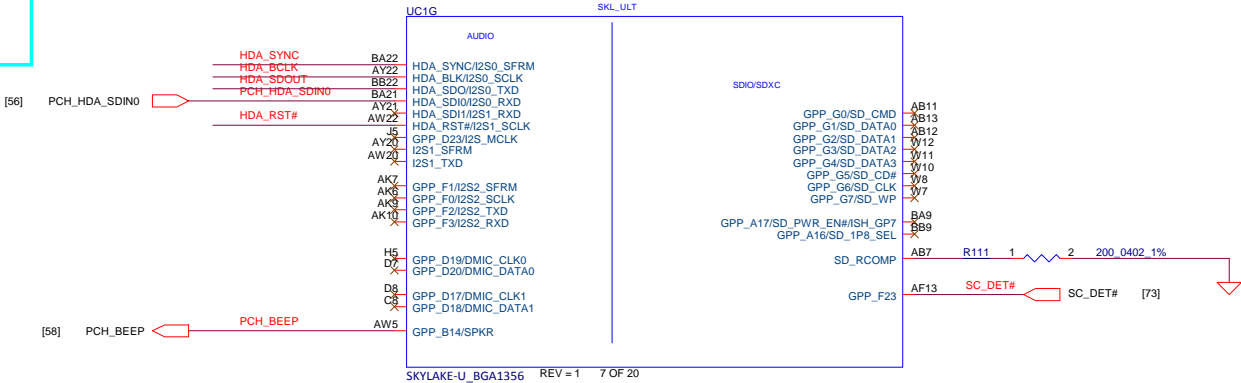
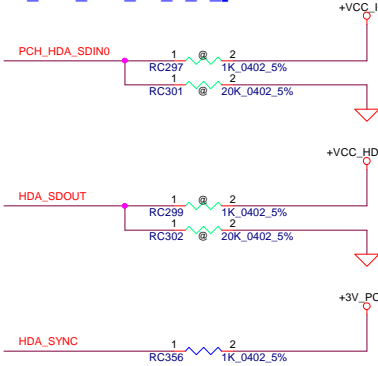
Need to check again?



GPP_B14, Internal PD 20K
No Reboot on TCO
Timer expiration
pull-up to VCC3.3 through a 1~8.2KΩ
resistor to disable this capability



Processor Strapping
543016_SKL_PDG_UY_1_0_pub
P780



Card Reader

WLAN

LAN

HDD

SSD(NGFF)

GPU

UC1H SKL_ULT

PCIe/USB3/SATA

SSIC / USB3

USB2

SKYLAKE-U_BGA1356 REV = 1 8 OF 20

On Board (Right-Front)

On Board (Right-Back)

DOCKING

S/B (AOU Port)

On Board (Right-Front)

On Board (Right-Back)

DOCKING

S/B (AOU Port)

SMART CARD

Finger Printer

BT

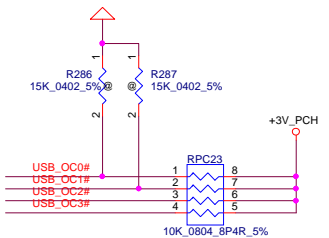
CAMERA

WWAN

Touch Panel

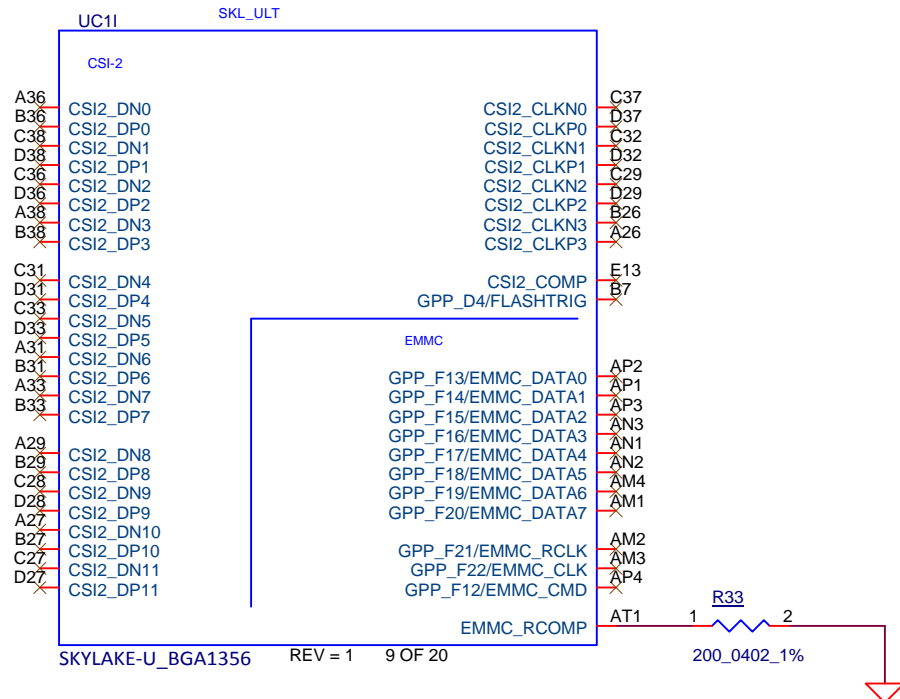
On Board (Right-Front)
S/B (AOU Port)


HDD_DEVSLP0 RC377 2 @ 1 10K 0402 5%
SSD_DEVSLP1 RC378 2 @ 1 10K 0402 5%



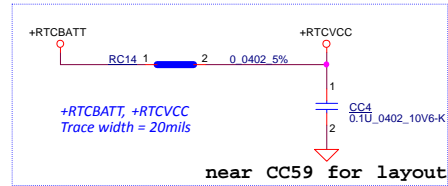
Pin.	USB3.0 Port NO.	USB2.0 Port NO.	Default Port Mapping
USB_OC0#	Port 1, 2	Port 0, 1	Port 0, 1
USB_OC1#	Port 4	Port 3	Port 2, 3
USB_OC2#	Unused.	Unused.	Port 4, 5
USB_OC3#	Unused.	Unused.	Port 6, 7

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2015/01/12				2016/01/12				SKL_PCIE/ SATA/ USB			
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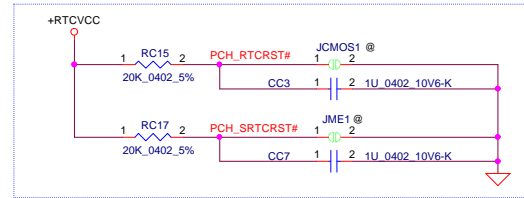


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		BL460_NM-A651									
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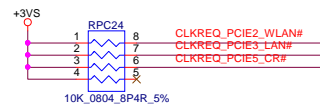
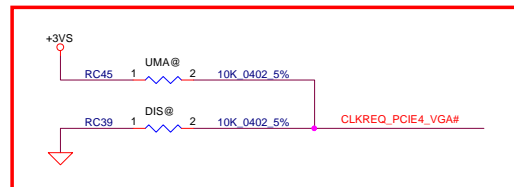
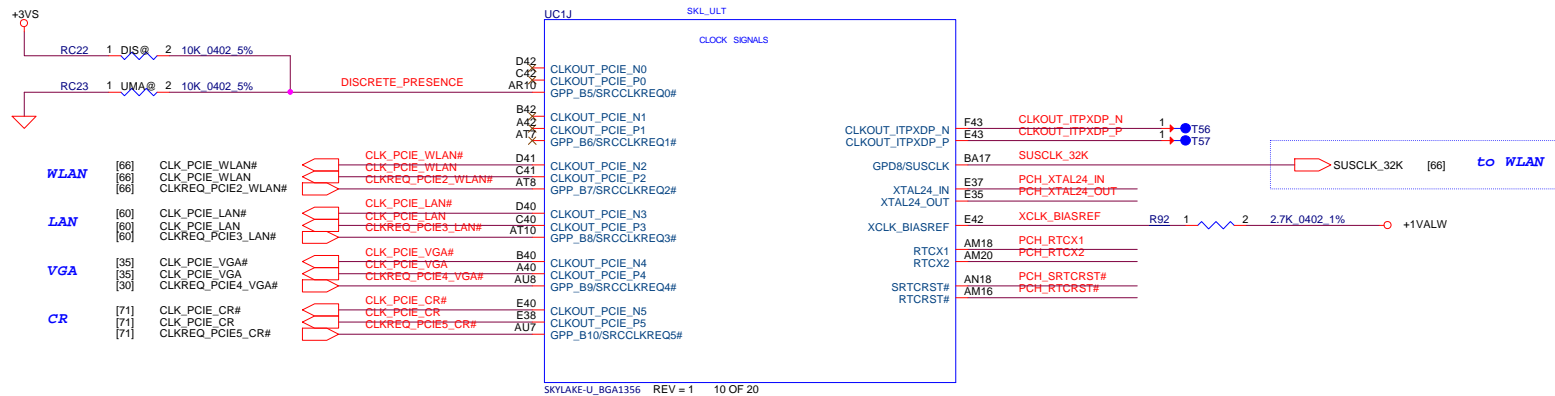
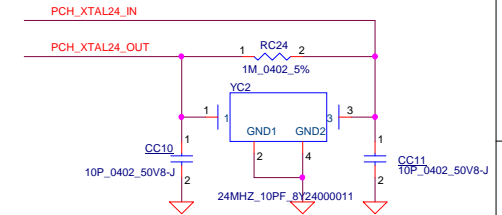
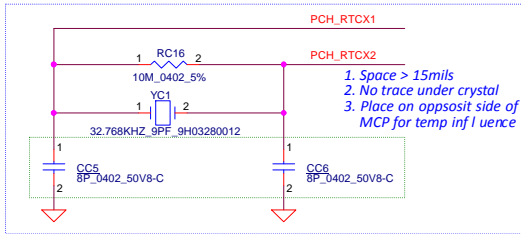
RTC External Circuit

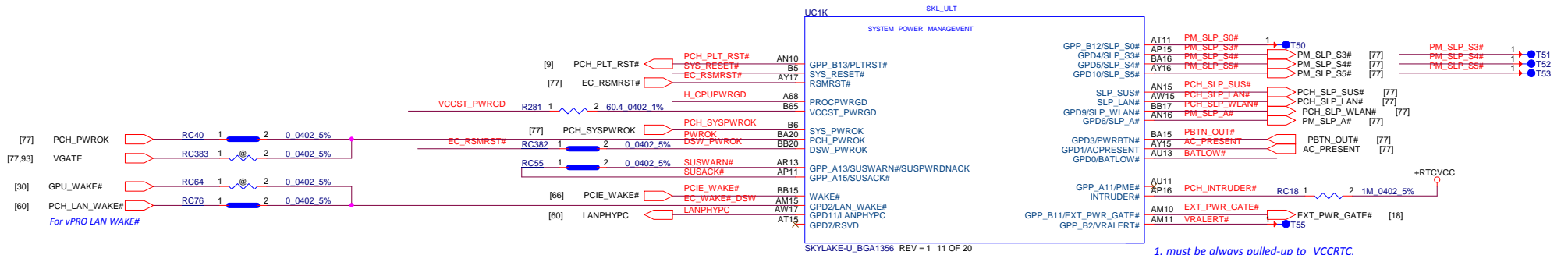


JCMOS, JME Set ting Need Undr DDR Dao

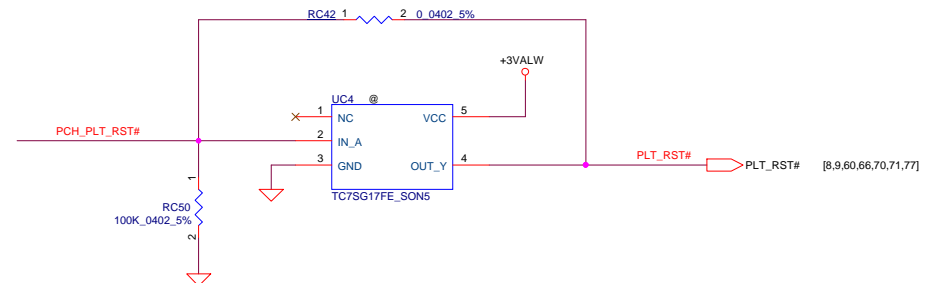
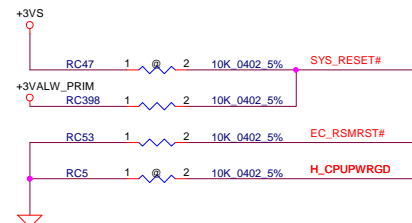
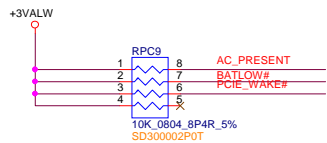


RTC Crystal

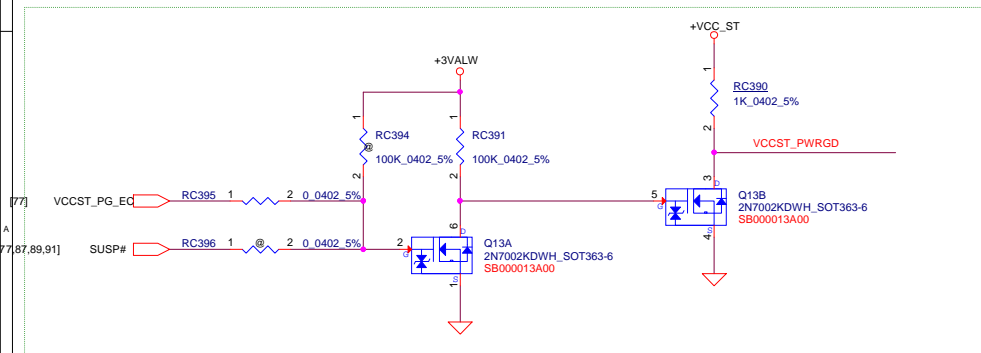




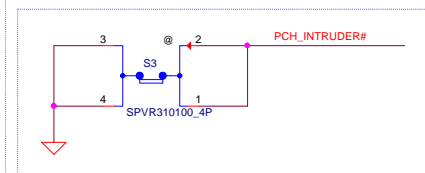
1. must be always pulled-up to VCCRTC.
2. 1 = Enable DSW 3.3V-to-1.05V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on product i on board.



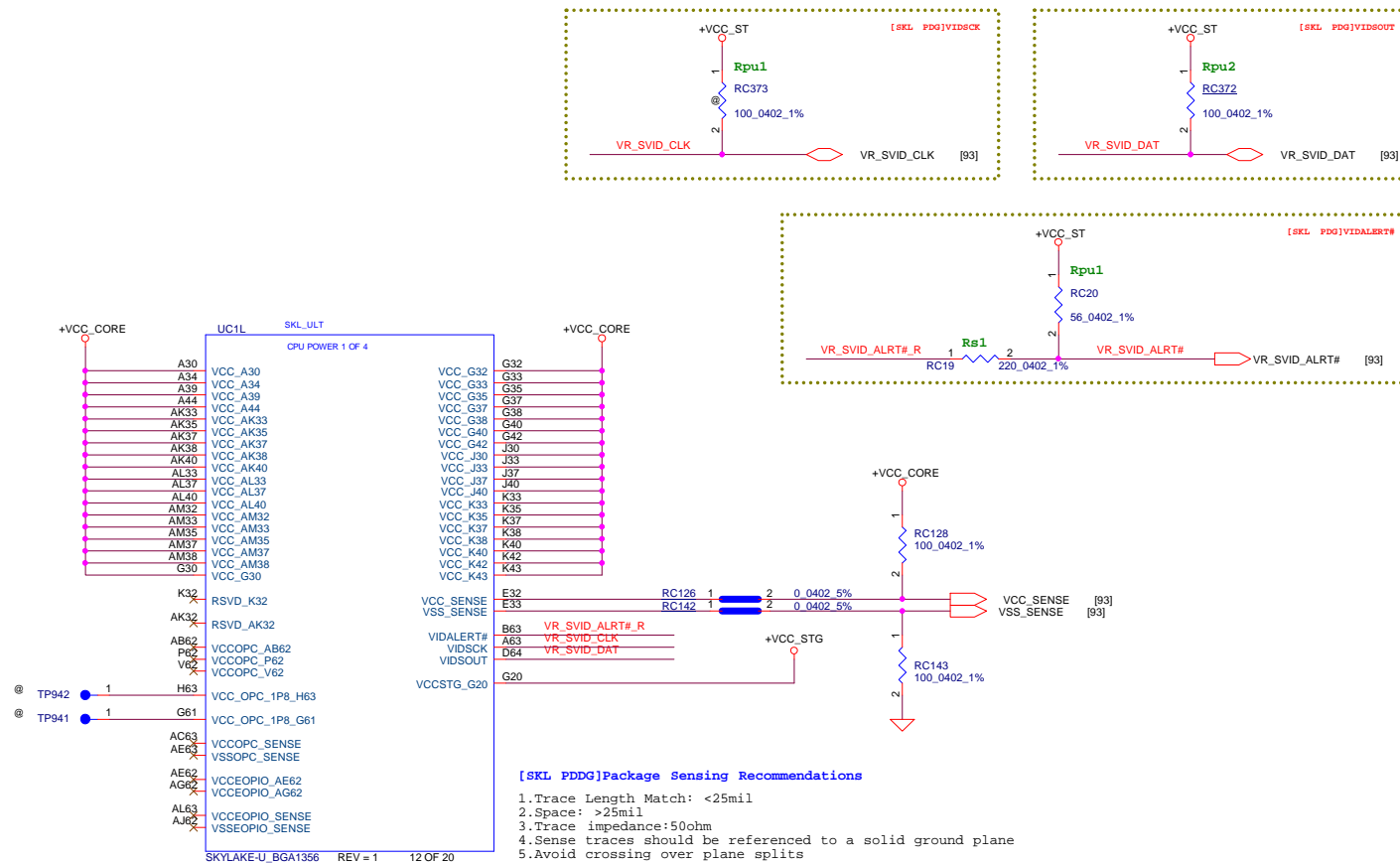
Reserved for HW control

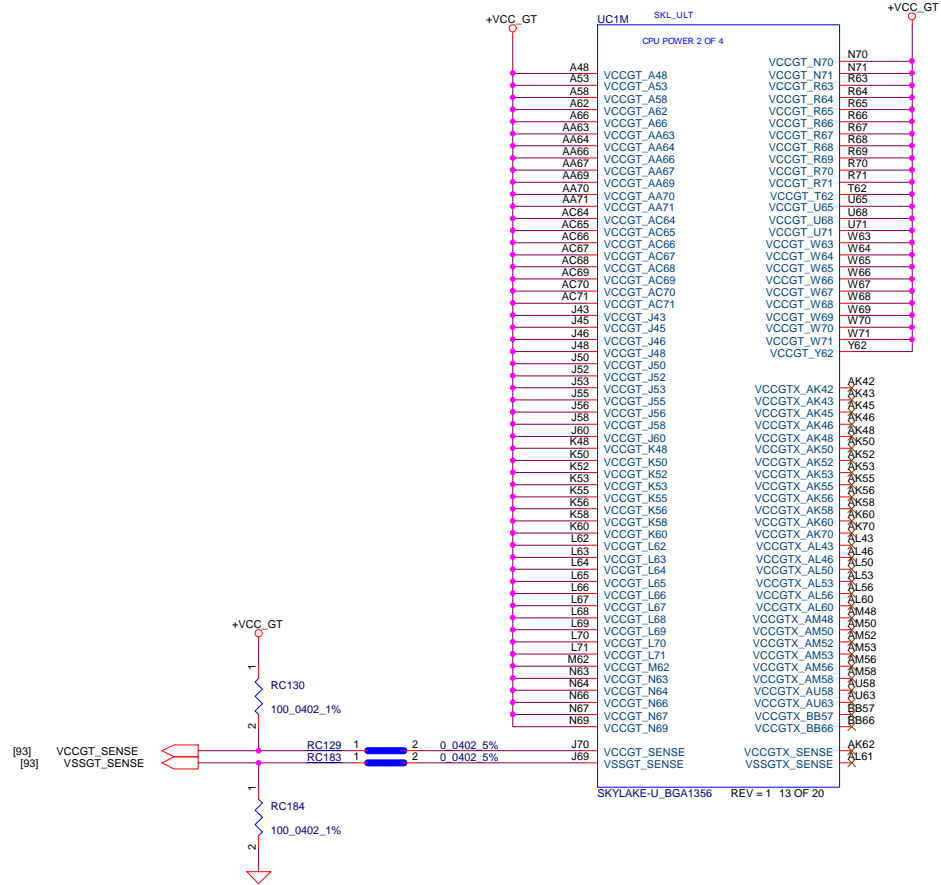


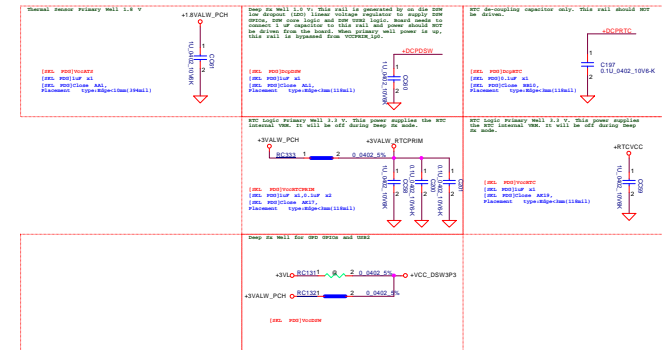
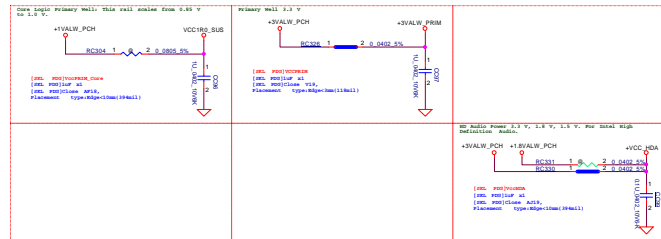
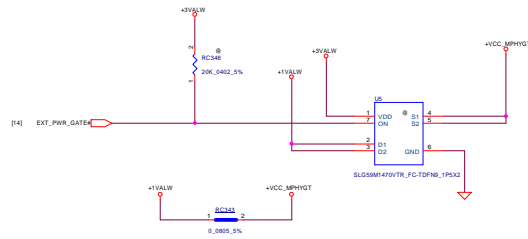
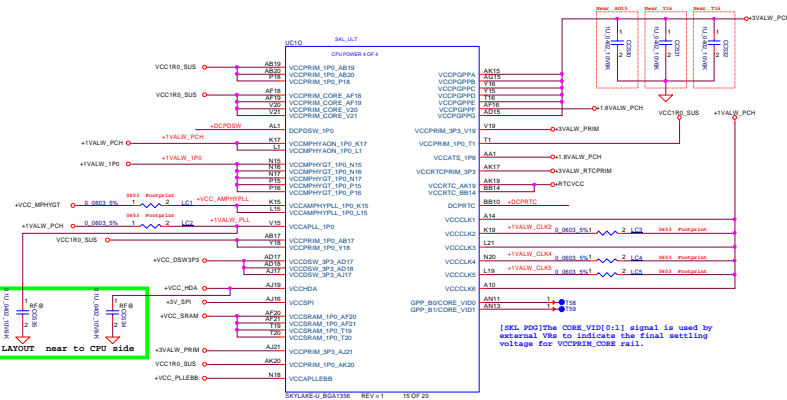
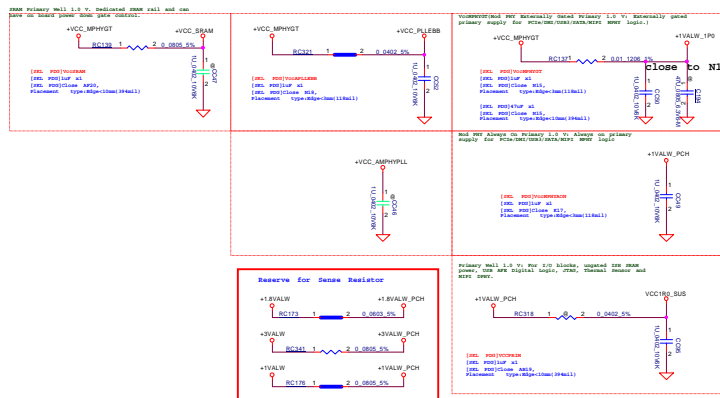
RTC clock debounce

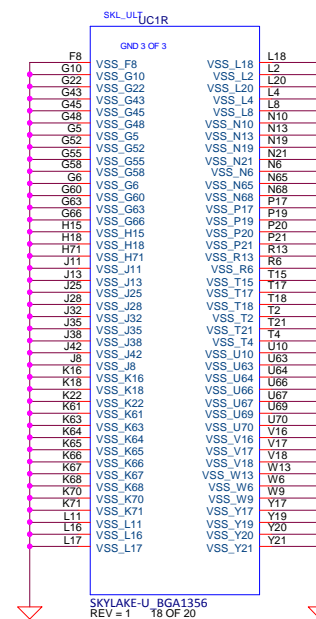
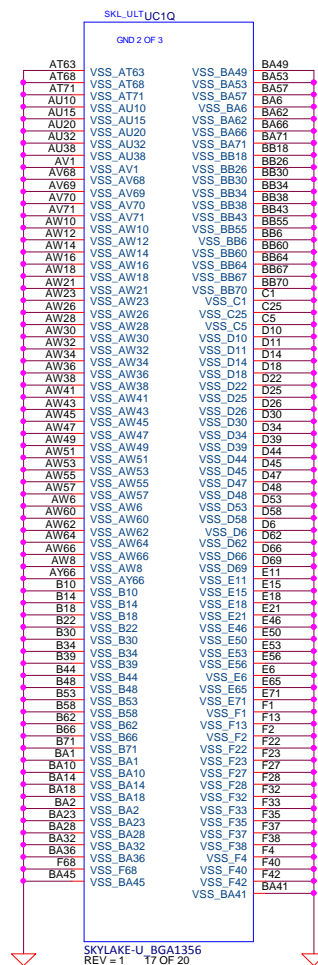
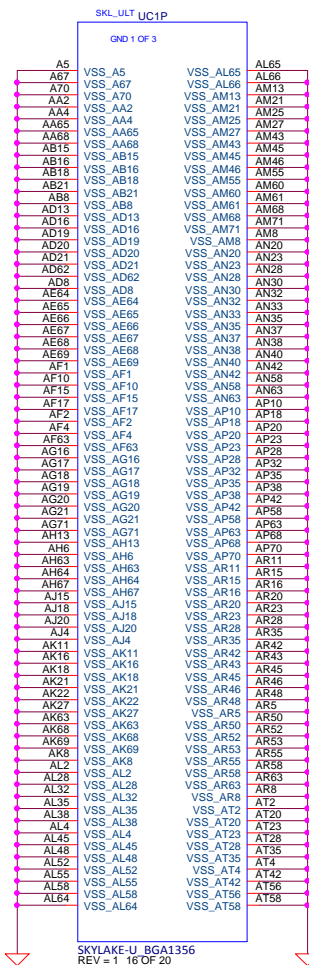



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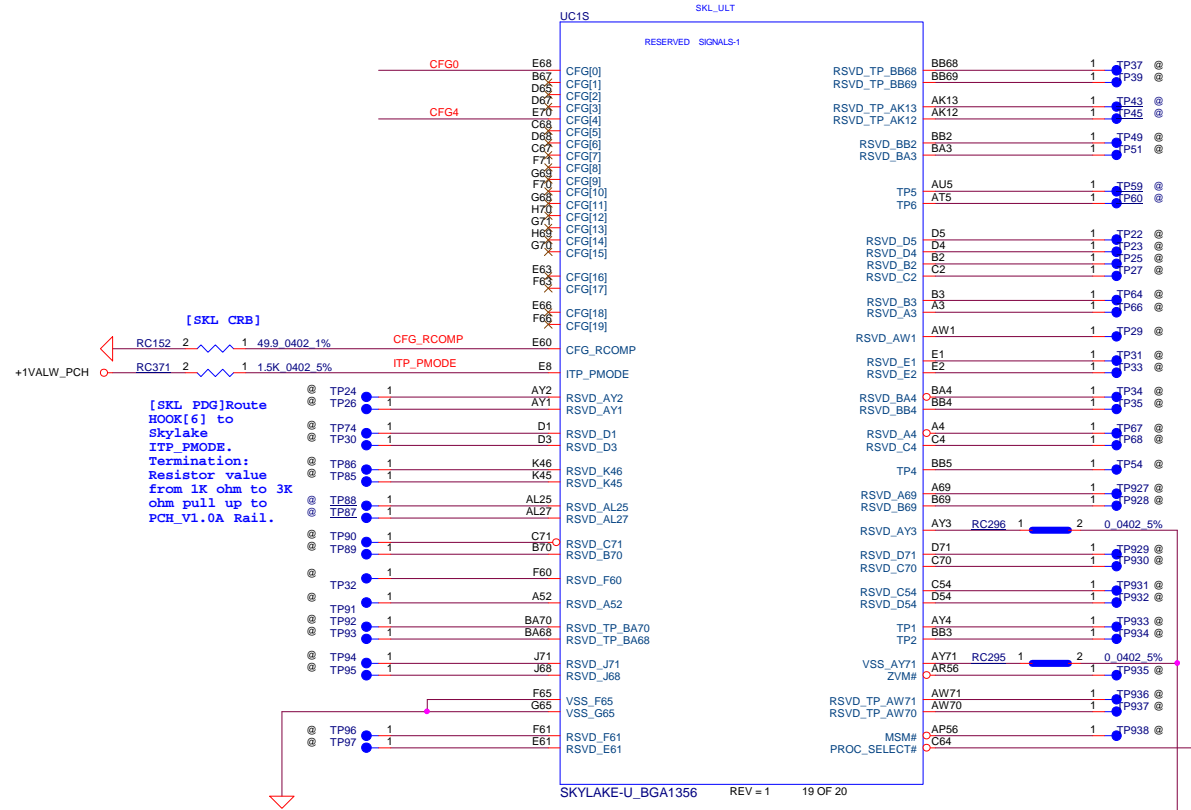




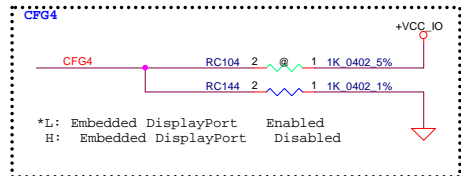
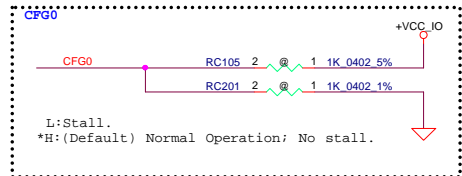




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[SKL_EDS]



TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted
1 : No Stall
0 : Stall

CFG4 : eDP Enable
1 : Disabled
0 : Enabled

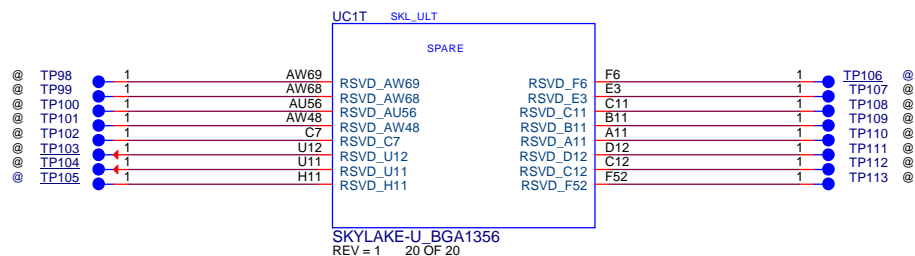
CFG9 : SVID Bus Communication
1 : Enabled
0 : Disabled


[SKL_EDS]Zero Voltage Mode:VCCOPC is fixed OPC VR output voltage of 1V, the processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal as shown below:

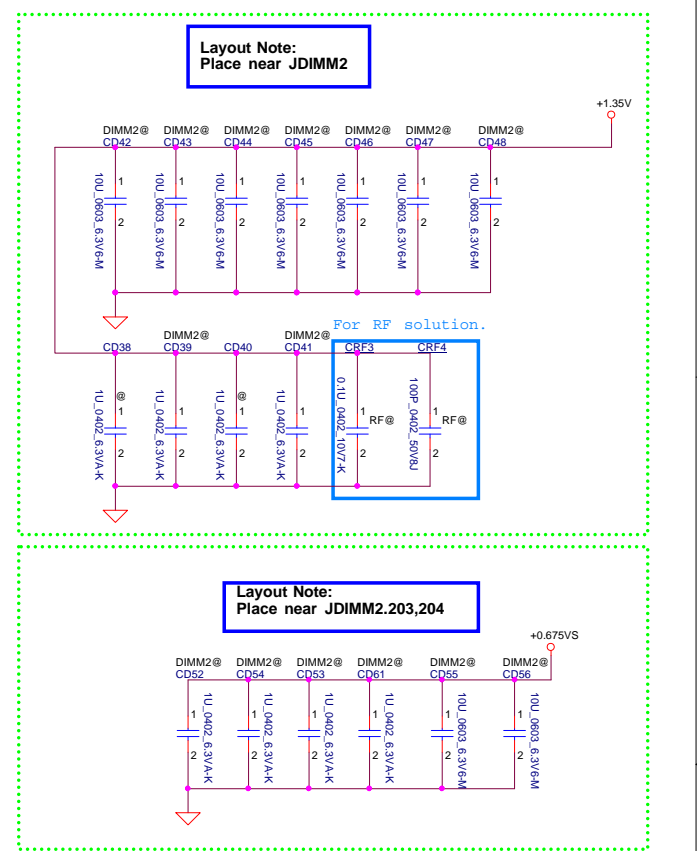
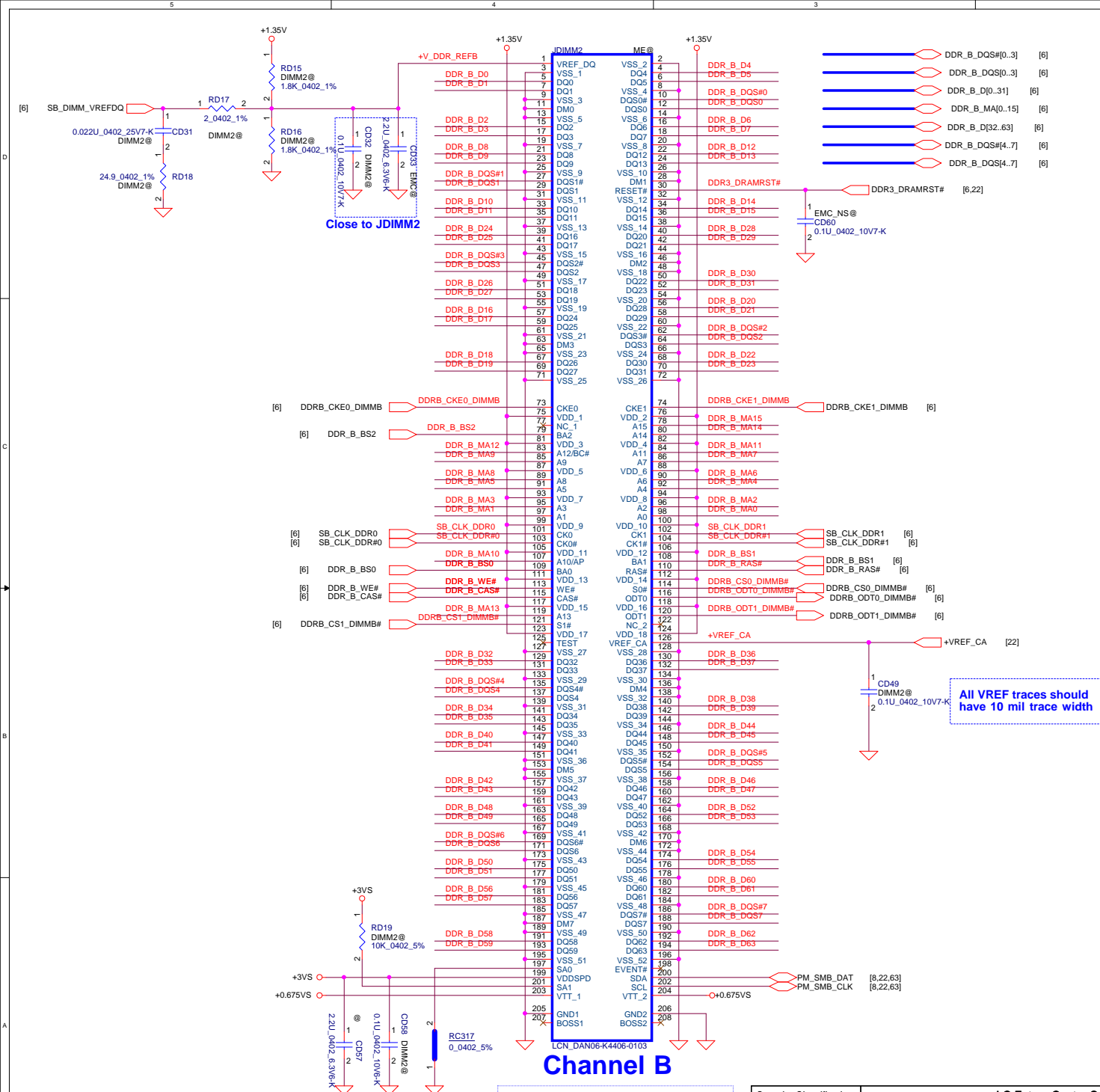
ZVM#	state	VCCOPC
0V		0V
1V		1V

[SKL_EDS]Minimum Speed Mode: VCCEOPIO can be connected to OPC VR in this case VCCEOPIO is fixed to 1V. The processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal . In order to achieve better power/performance it is recommended to use a separate VR for VCCEOPIO in this case VCCEOPIO is configurable to 0.8V/1V. The processor drives the VR to set VCCEOPIO value(0.8V/1V) using MSM# signal, based on the required bandwidth for the EOPIO interface as shown below:

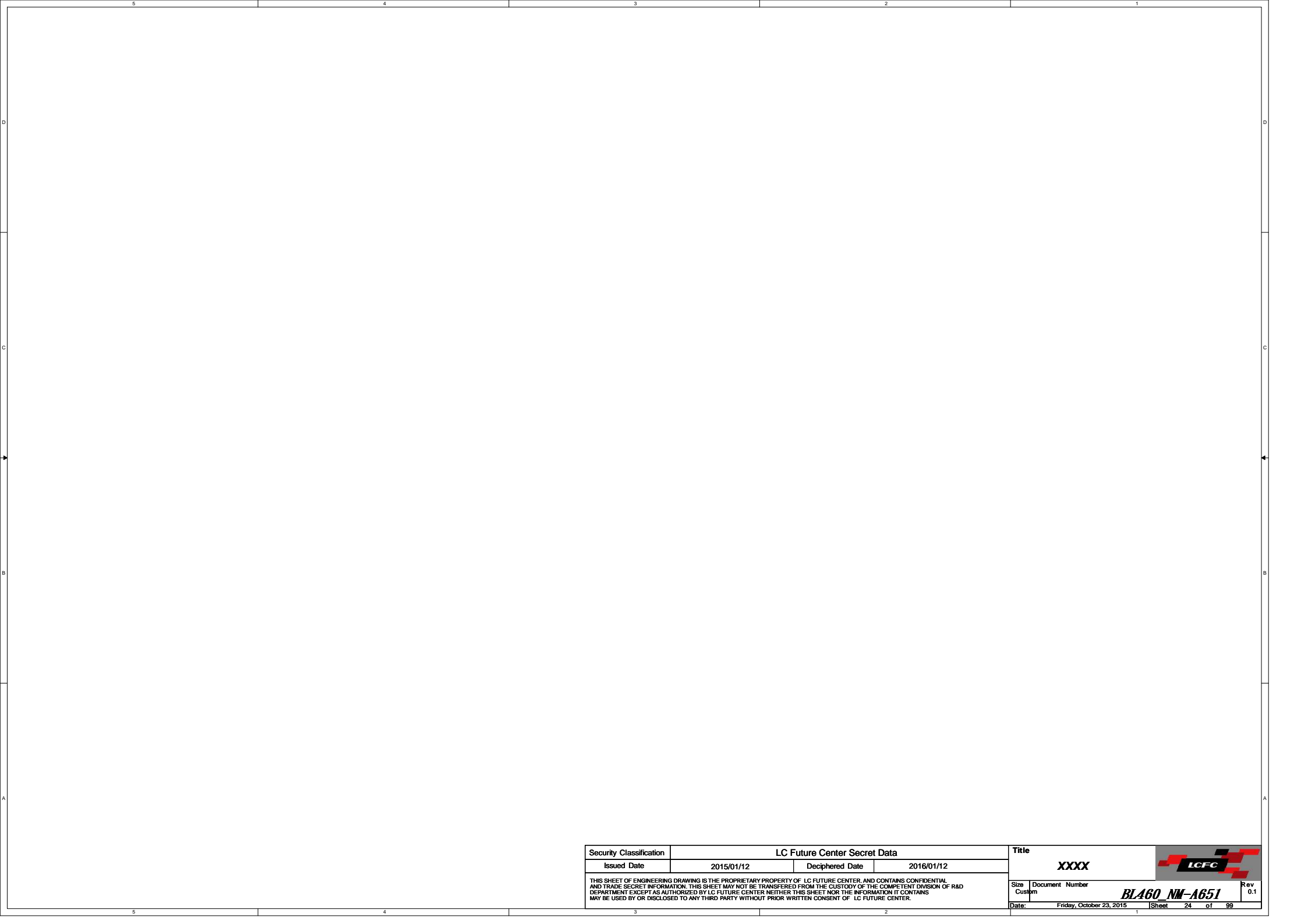
ZVM#	state	MSM#	state	VCCEOPIO
0V		X		0V
1V		0V		0.8V
1V		1V		1V




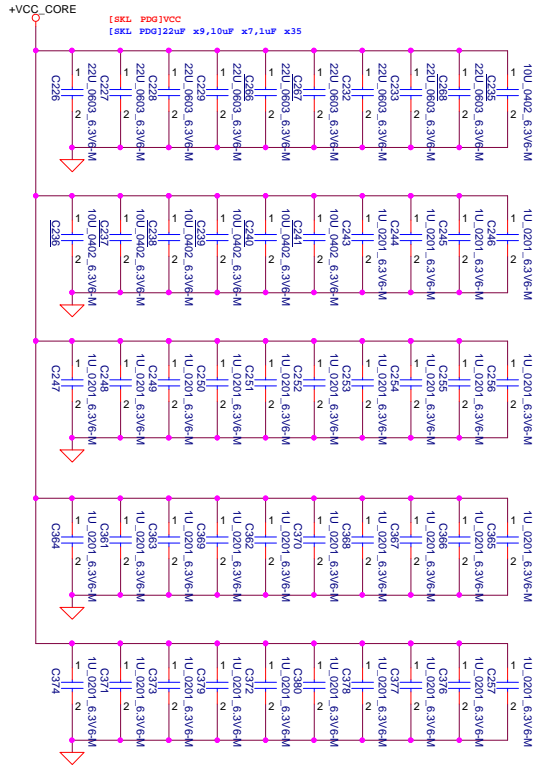
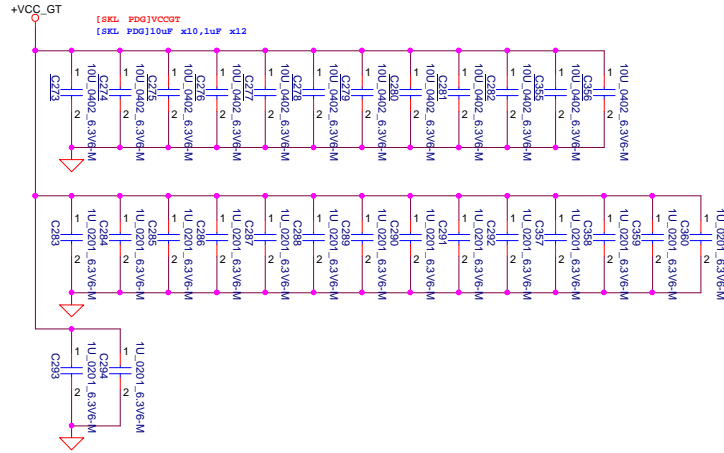
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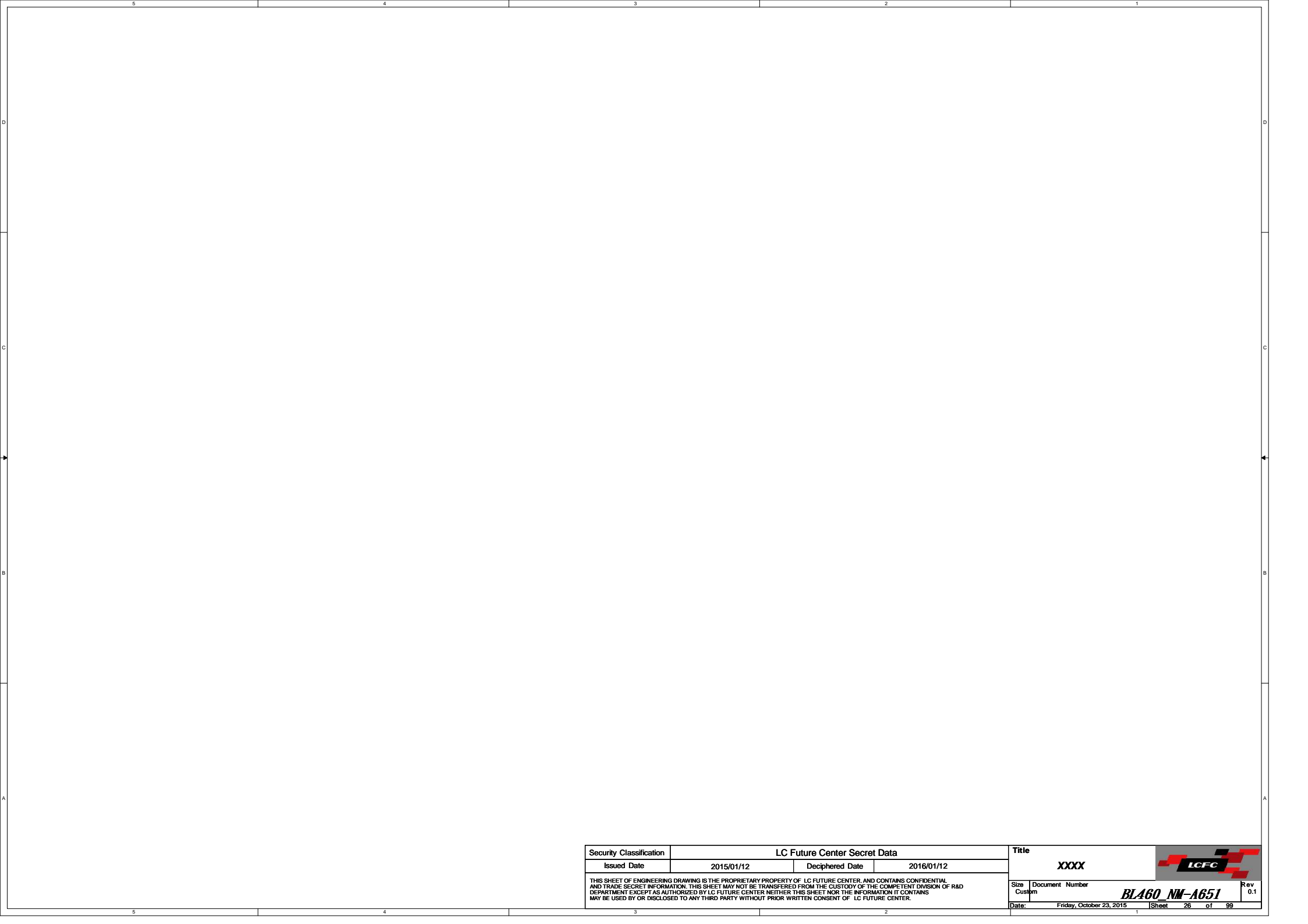



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				Date:	Friday, October 23, 2015	Sheet	23 of 99

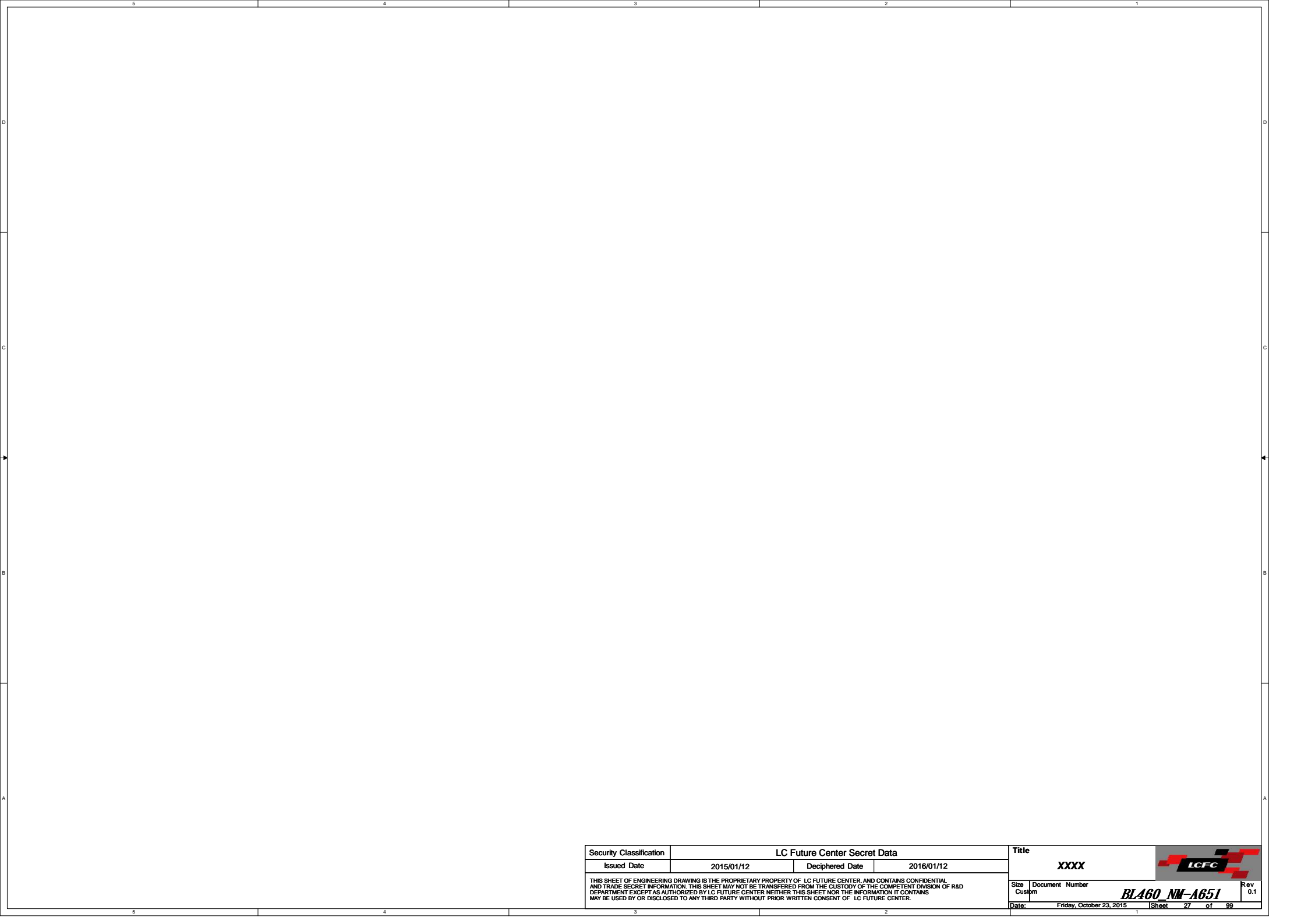



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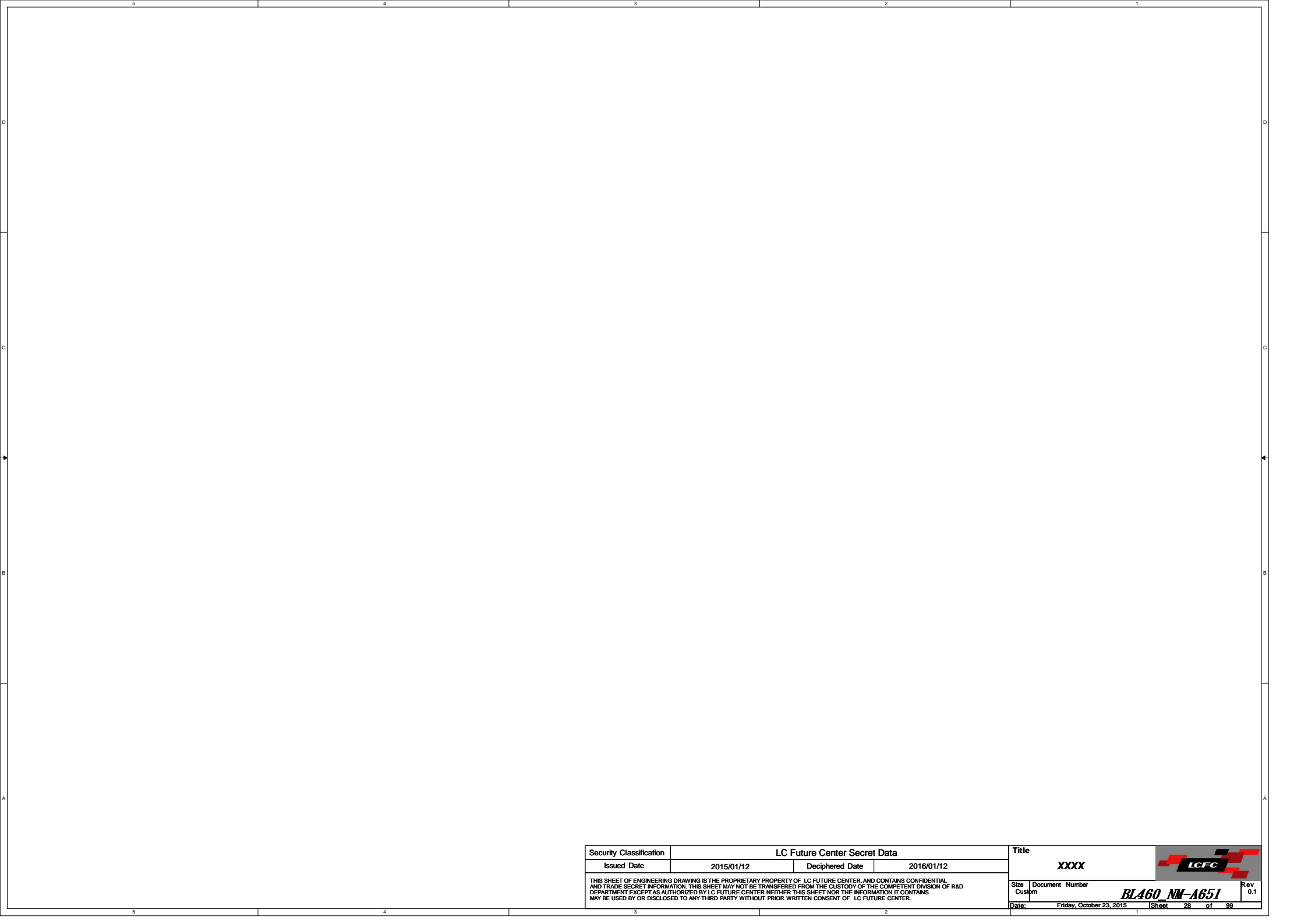





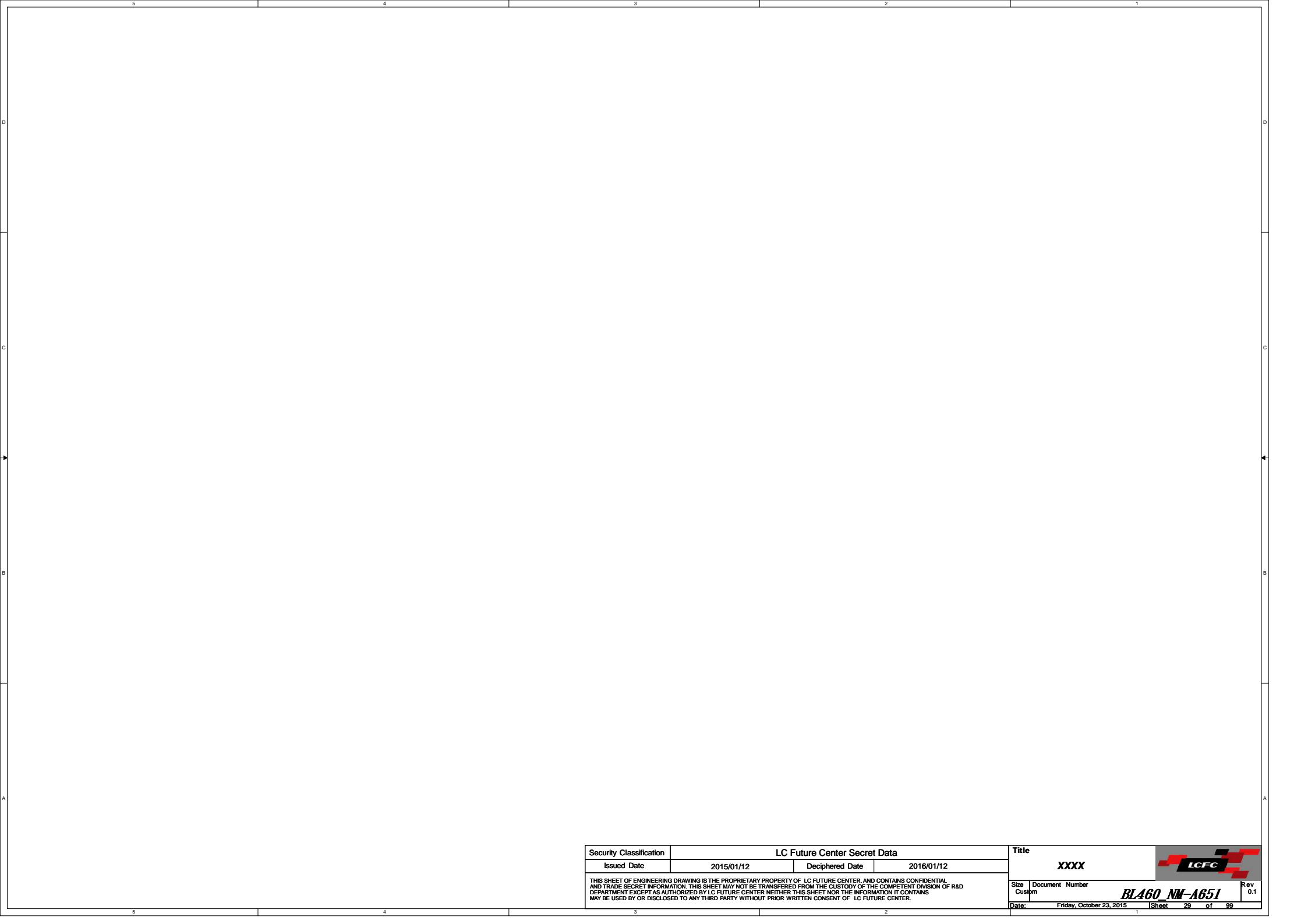
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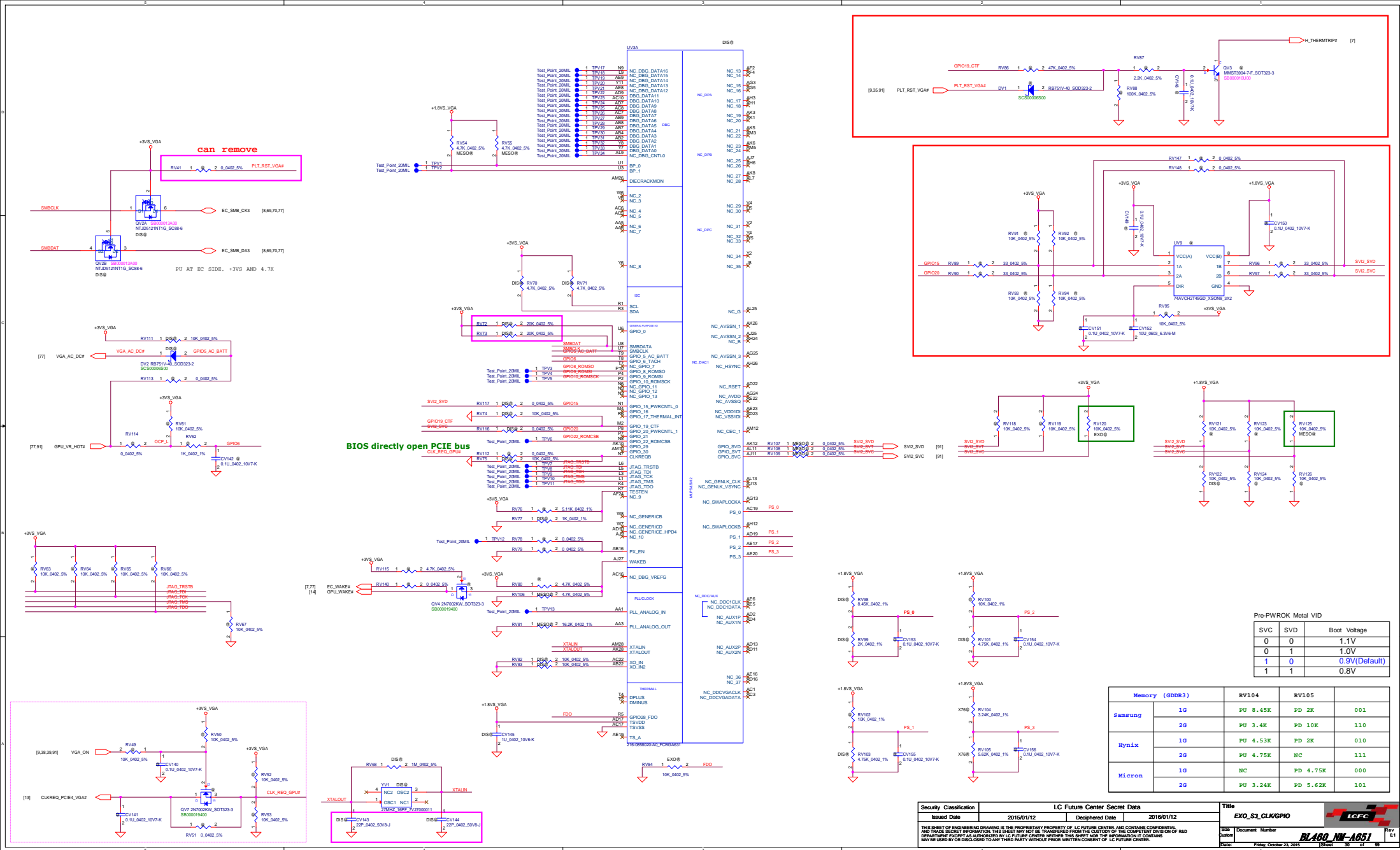
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						Date:	Friday, October 23, 2015	Sheet	27 of 99

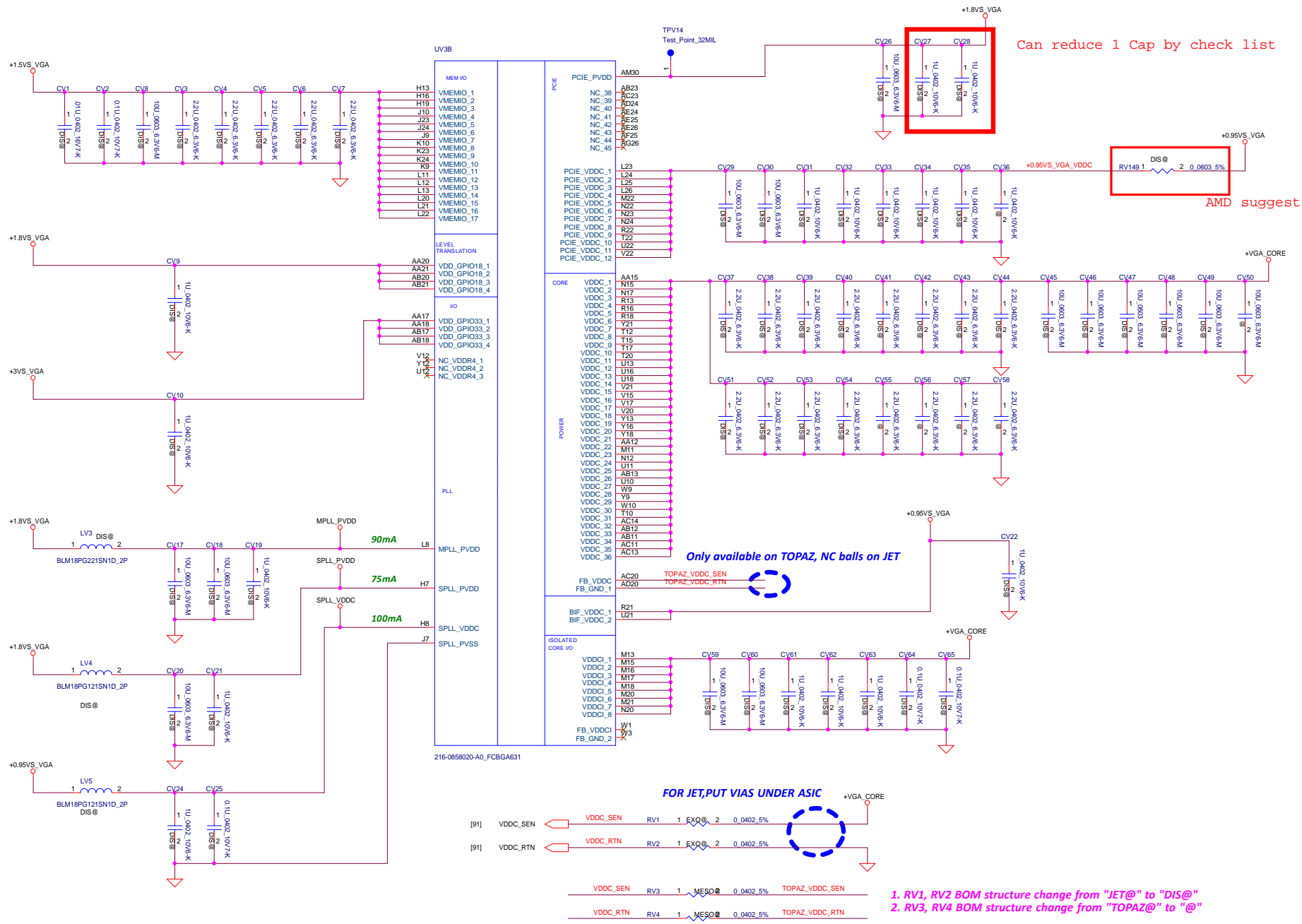



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				Date:	Friday, October 23, 2015	Sheet 28 of 99

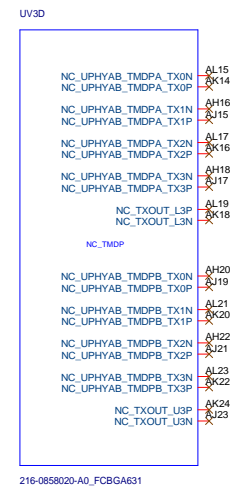


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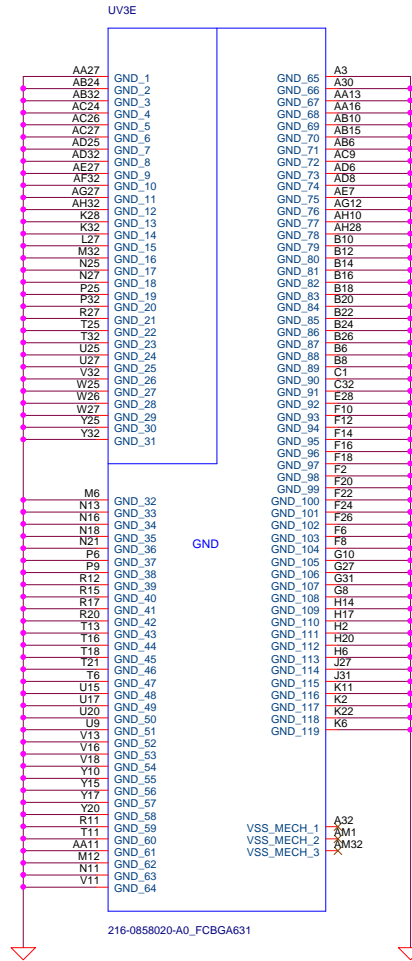


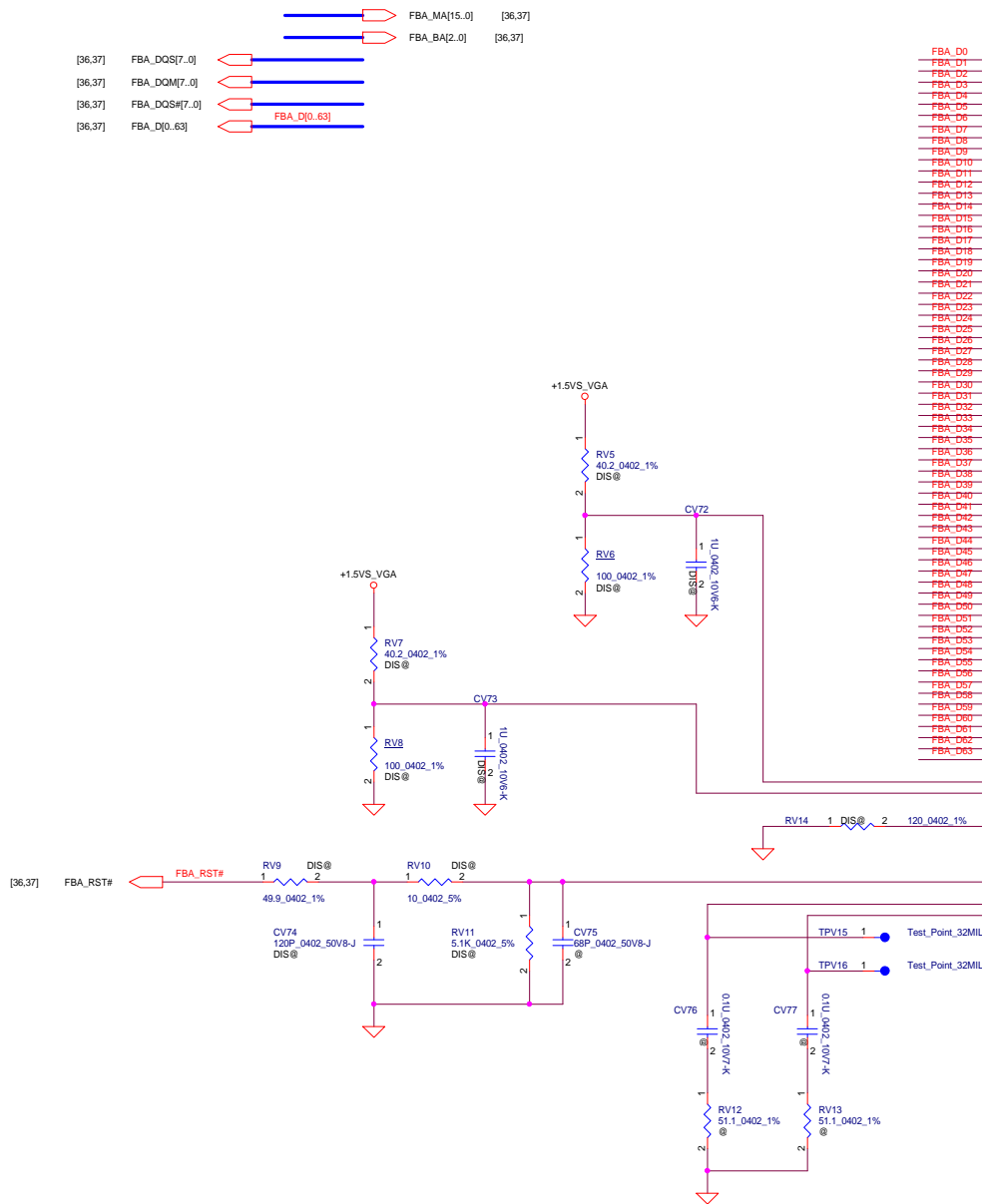
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ASIC Ball	Topaz	Jet
U1	BP_0	NC
U3	BP_1	NC
AM26	DIECRACKMON	NC
Y11	NC	DBG_DATA13
AE9	NC	DBG_DATA14
L9	NC	DBG_DATA15
N9	NC	DBG_DATA16
AE8	NC	DBG_DATA12
AL9	NC	DBG_CNTL0
H13, H16, H19, J10 J23, J24, J9, K10 K23, K24, K9, L11 L12, L13, L20, L21 L22	VMEMIO	VDDR1
AA17, AA18 AB17, AB18	VDD_GPIO33	VDDR3
AA20, AA21 AB20, AB21	VDD_GPIO18	VDD_CT

	Bits5	Bits4	Bits3	Bits2	Bits1
PS0	1	1	0	0	1
PS1	1	1	0	0	0
PS2	0	0	0	0	0
PS3	1	1	?	?	?





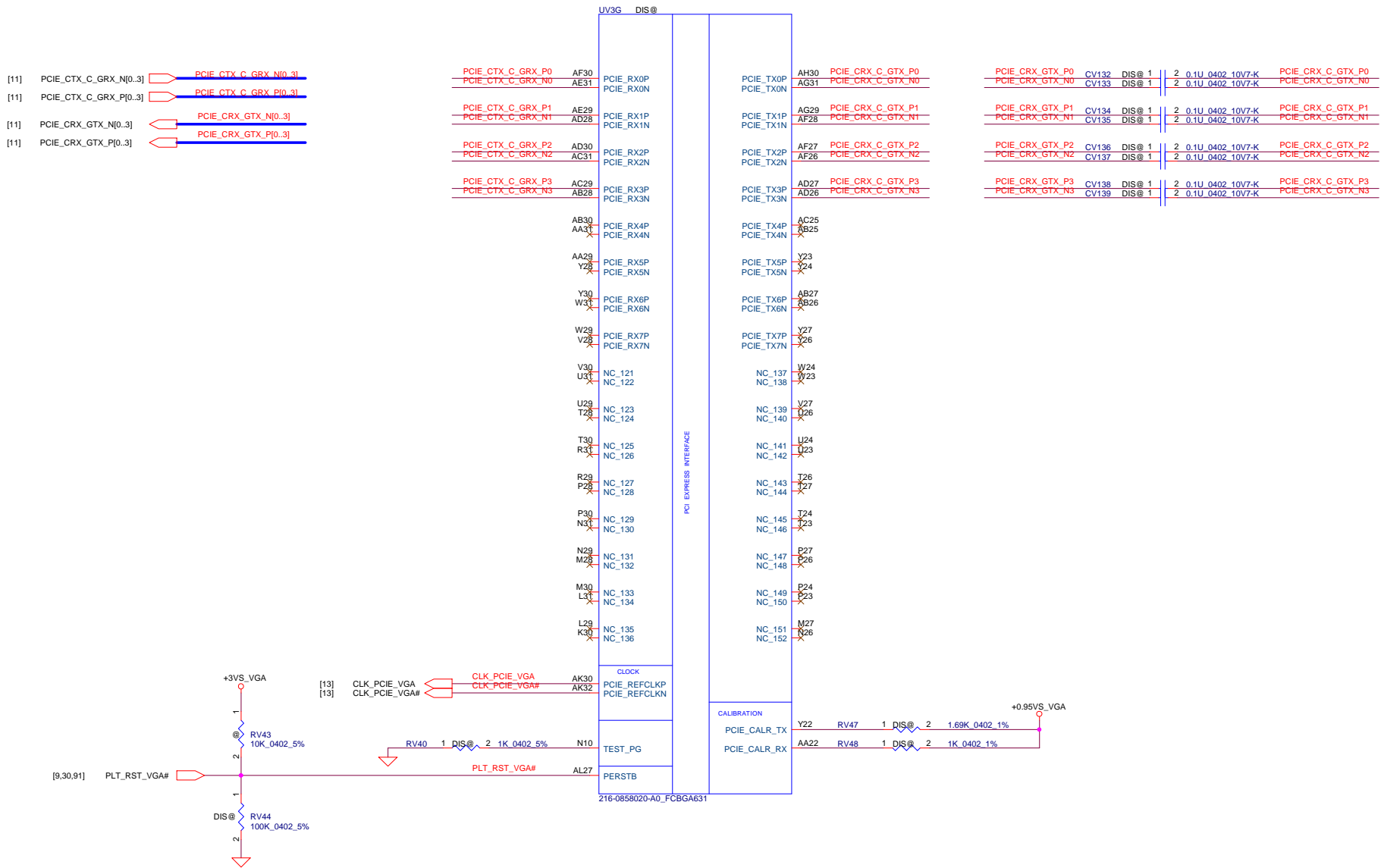
UV3F

FBA_D0	K27	DQA0_0
FBA_D1	D29	DQA0_1
FBA_D2	H30	DQA0_2
FBA_D3	H32	DQA0_3
FBA_D4	G29	DQA0_4
FBA_D5	F28	DQA0_5
FBA_D6	F32	DQA0_6
FBA_D7	F30	DQA0_7
FBA_D8	C30	DQA0_8
FBA_D9	F27	DQA0_9
FBA_D10	A28	DQA0_10
FBA_D11	C28	DQA0_11
FBA_D12	E27	DQA0_12
FBA_D13	G26	DQA0_13
FBA_D14	D26	DQA0_14
FBA_D15	F26	DQA0_15
FBA_D16	A26	DQA0_16
FBA_D17	C26	DQA0_17
FBA_D18	E26	DQA0_18
FBA_D19	D24	DQA0_19
FBA_D20	E23	DQA0_20
FBA_D21	F23	DQA0_21
FBA_D22	D22	DQA0_22
FBA_D23	F21	DQA0_23
FBA_D24	E21	DQA0_24
FBA_D25	D20	DQA0_25
FBA_D26	F19	DQA0_26
FBA_D27	A19	DQA0_27
FBA_D28	D18	DQA0_28
FBA_D29	F17	DQA0_29
FBA_D30	A17	DQA0_30
FBA_D31	C17	DQA0_31
FBA_D32	E17	DQA0_32
FBA_D33	D16	DQA0_33
FBA_D34	F15	DQA0_34
FBA_D35	A15	DQA0_35
FBA_D36	D14	DQA0_36
FBA_D37	F13	DQA0_37
FBA_D38	A13	DQA0_38
FBA_D39	C13	DQA0_39
FBA_D40	E11	DQA0_40
FBA_D41	A11	DQA0_41
FBA_D42	C11	DQA0_42
FBA_D43	F11	DQA0_43
FBA_D44	A9	DQA0_44
FBA_D45	C9	DQA0_45
FBA_D46	F9	DQA0_46
FBA_D47	D8	DQA0_47
FBA_D48	E7	DQA0_48
FBA_D49	A7	DQA0_49
FBA_D50	C7	DQA0_50
FBA_D51	F7	DQA0_51
FBA_D52	A5	DQA0_52
FBA_D53	E5	DQA0_53
FBA_D54	C3	DQA0_54
FBA_D55	F1	DQA0_55
FBA_D56	G7	DQA0_56
FBA_D57	G6	DQA0_57
FBA_D58	G1	DQA0_58
FBA_D59	G3	DQA0_59
FBA_D60	J6	DQA0_60
FBA_D61	J1	DQA0_61
FBA_D62	J5	DQA0_62
FBA_D63	J6	DQA0_63

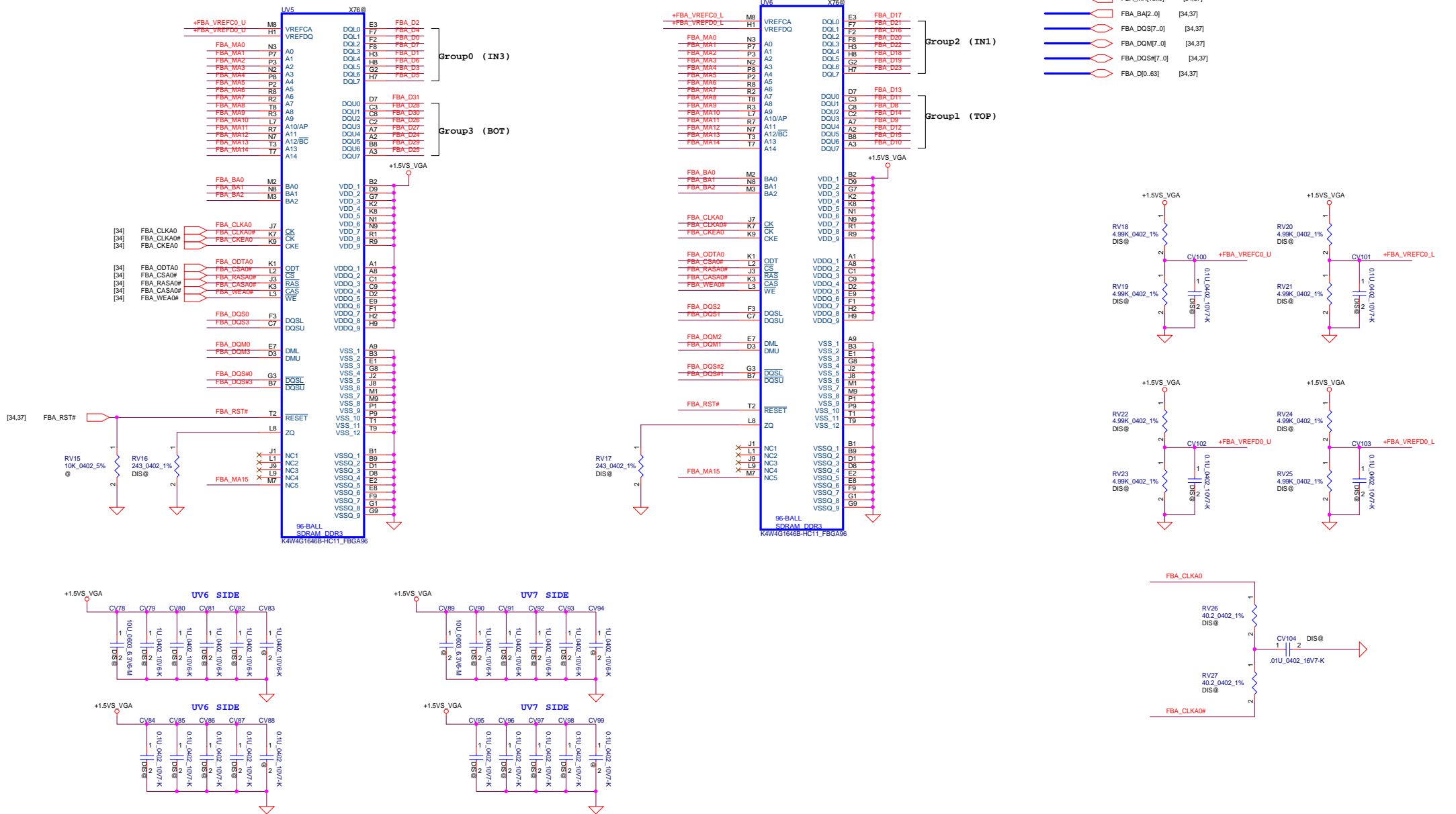
MEMORY INTERFACE


MAA0_0	K17	FBA_MA0
MAA0_1	H20	FBA_MA1
MAA0_2	G23	FBA_MA2
MAA0_3	H24	FBA_MA3
MAA0_4	H24	FBA_MA4
MAA0_5	J19	FBA_MA5
MAA0_6	K19	FBA_MA6
MAA0_7	G20	FBA_MA7
MAA0_8	L17	FBA_MA8
MAA0_9	L17	FBA_MA9
MAA1_0	J14	FBA_MA10
MAA1_1	K14	FBA_MA11
MAA1_2	J11	FBA_MA12
MAA1_3	J13	FBA_MA13
MAA1_4	H11	FBA_MA14
MAA1_5	G11	FBA_MA15
MAA1_6	J16	FBA_MA16
MAA1_7	L15	FBA_MA17
MAA1_8	G14	FBA_MA18
MAA1_9	L16	FBA_MA19
WCKA0_0	E32	FBA_QM0
WCKA0_1	E30	FBA_QM1
WCKA0_2	A21	FBA_QM2
WCKA0_3	C21	FBA_QM3
WCKA0_4	E13	FBA_QM4
WCKA0_5	D12	FBA_QM5
WCKA0_6	E3	FBA_QM6
WCKA0_7	F4	FBA_QM7
WCKA0_8	H28	FBA_QM8
WCKA0_9	C27	FBA_QM9
WCKA0_10	A23	FBA_QM10
WCKA0_11	E19	FBA_QM11
WCKA0_12	E15	FBA_QM12
WCKA0_13	D10	FBA_QM13
WCKA0_14	D6	FBA_QM14
WCKA0_15	G5	FBA_QM15
WCKA0_16	H27	FBA_QM16
WCKA0_17	A27	FBA_QM17
WCKA0_18	C23	FBA_QM18
WCKA0_19	C19	FBA_QM19
WCKA0_20	C15	FBA_QM20
WCKA0_21	E9	FBA_QM21
WCKA0_22	C5	FBA_QM22
WCKA0_23	H4	FBA_QM23
WCKA0_24	L18	FBA_QM24
WCKA0_25	K16	FBA_QM25
WCKA0_26	H26	FBA_QM26
WCKA0_27	H25	FBA_QM27
WCKA0_28	G9	FBA_QM28
WCKA0_29	H9	FBA_QM29
WCKA0_30	G22	FBA_QM30
WCKA0_31	G17	FBA_QM31
WCKA0_32	G19	FBA_QM32
WCKA0_33	G16	FBA_QM33
WCKA0_34	H22	FBA_QM34
WCKA0_35	X2	FBA_QM35
WCKA0_36	G13	FBA_QM36
WCKA0_37	X13	FBA_QM37
WCKA0_38	K20	FBA_QM38
WCKA0_39	J17	FBA_QM39
WCKA0_40	G25	FBA_QM40
WCKA0_41	H10	FBA_QM41

FBA_ODTA0	[36]
FBA_ODTA1	[37]
FBA_CLKA0	[36]
FBA_CLKA1	[37]
FBA_RASA0	[36]
FBA_RASA1	[37]
FBA_CASA0	[36]
FBA_CASA1	[37]
FBA_CSA0	[36]
FBA_CSA1	[37]
FBA_CKEA0	[36]
FBA_CKEA1	[37]
FBA_WEA0	[36]
FBA_WEA1	[37]

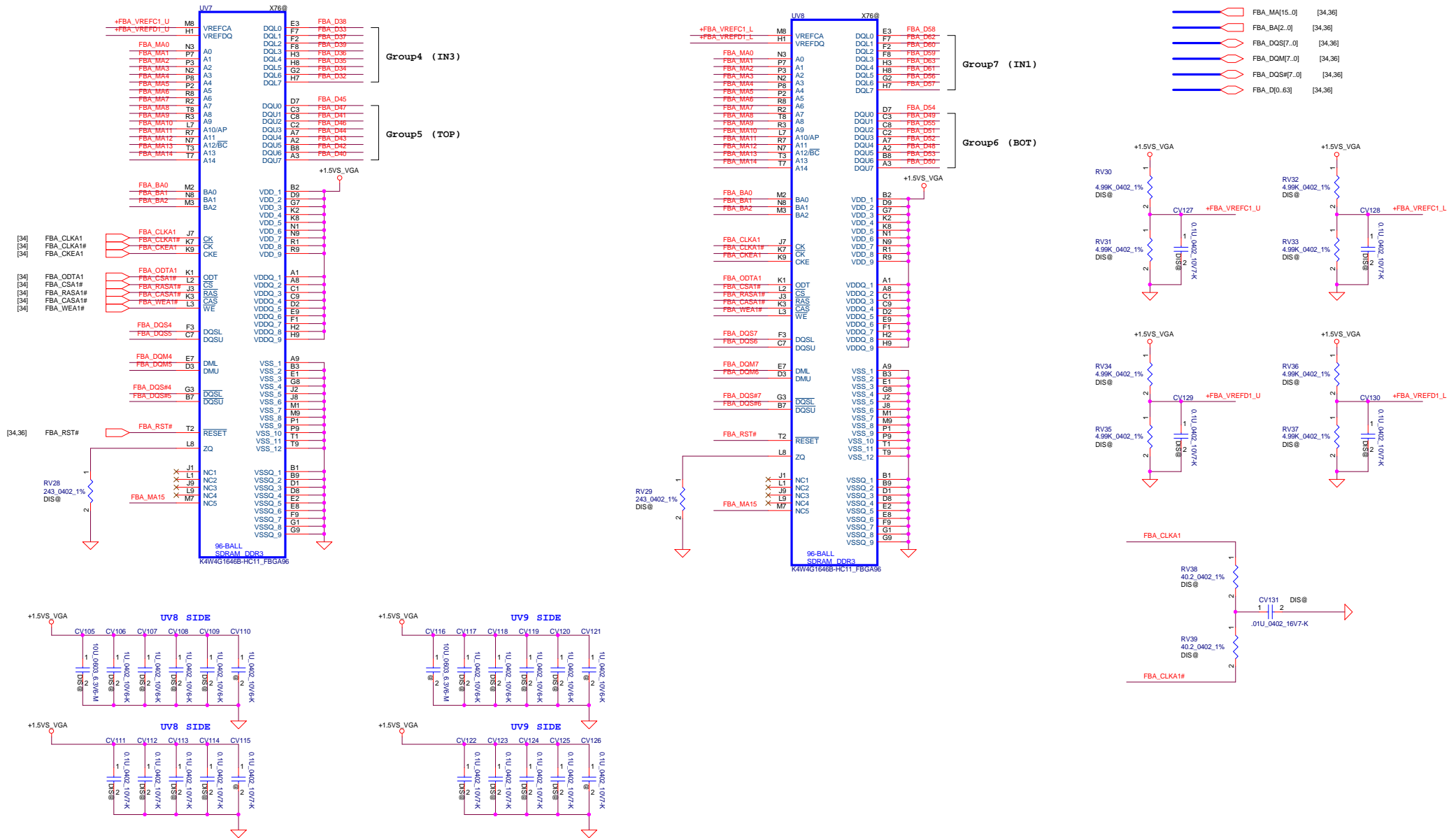


Memory Partition A - Lower 32 bits

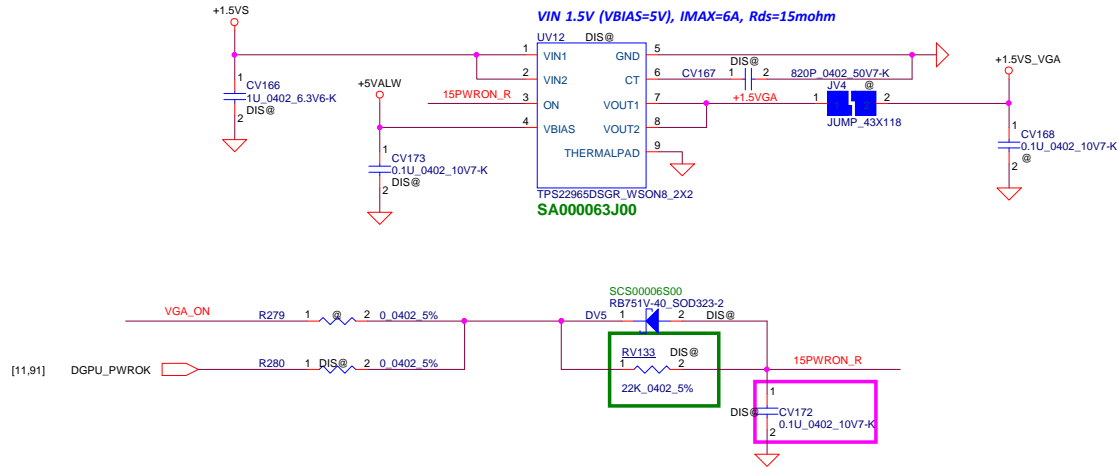


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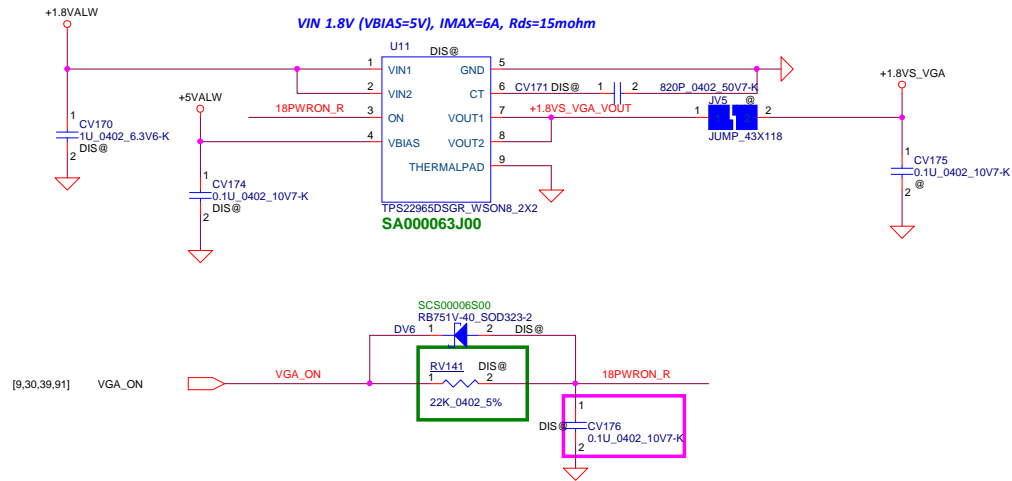
Memory Partition A - Upper 32 bits



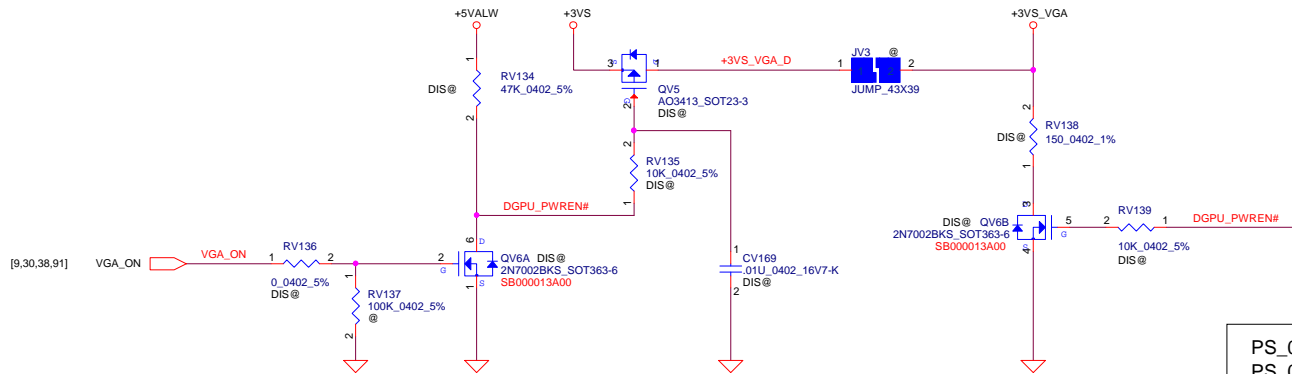
+1.5VS to +1.5VS_VGA



+1.8VALW to +1.8VS_VGA

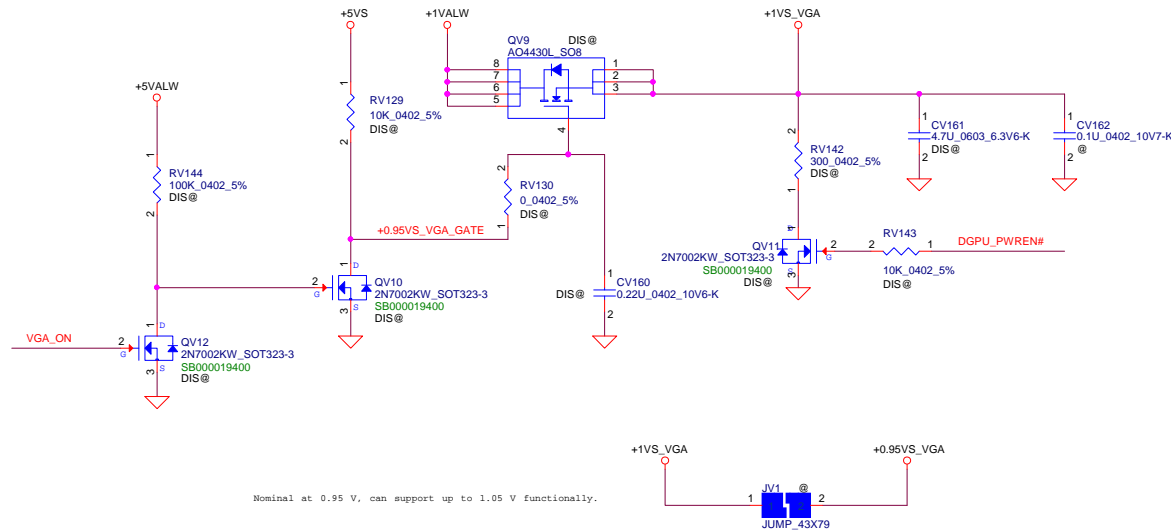


+3VS to +3VS_VGA




MLPS	Bit				
	5	4	3	2	1
PS_0[5:1]	1	1	0	0	1
PS_1[5:1]	1	1	0	0	0
PS_2[5:1]	1	1	0	0	0
PS_3[5:1]	1	1	X	X	X

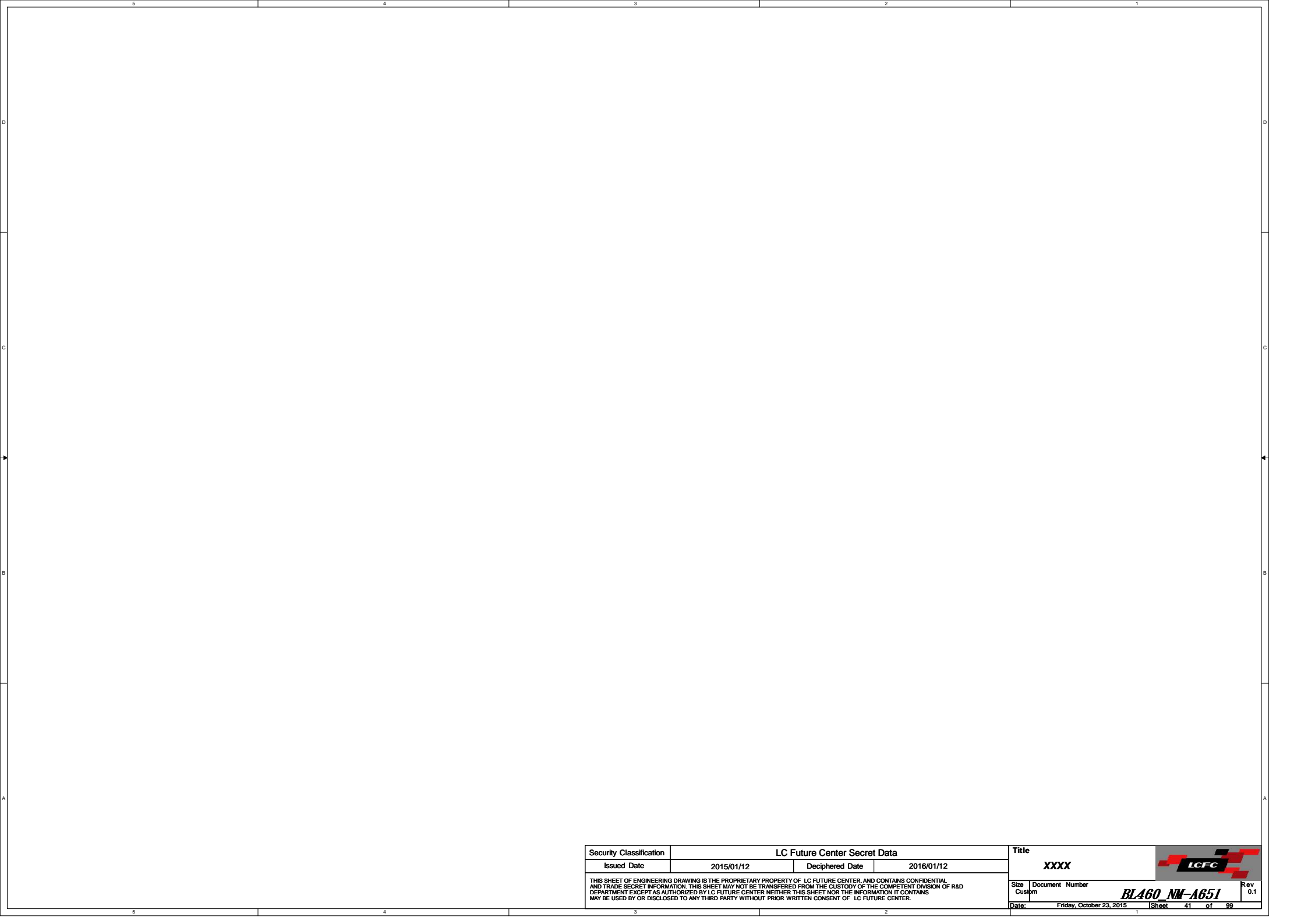
+1VALW to +1VS_VGA




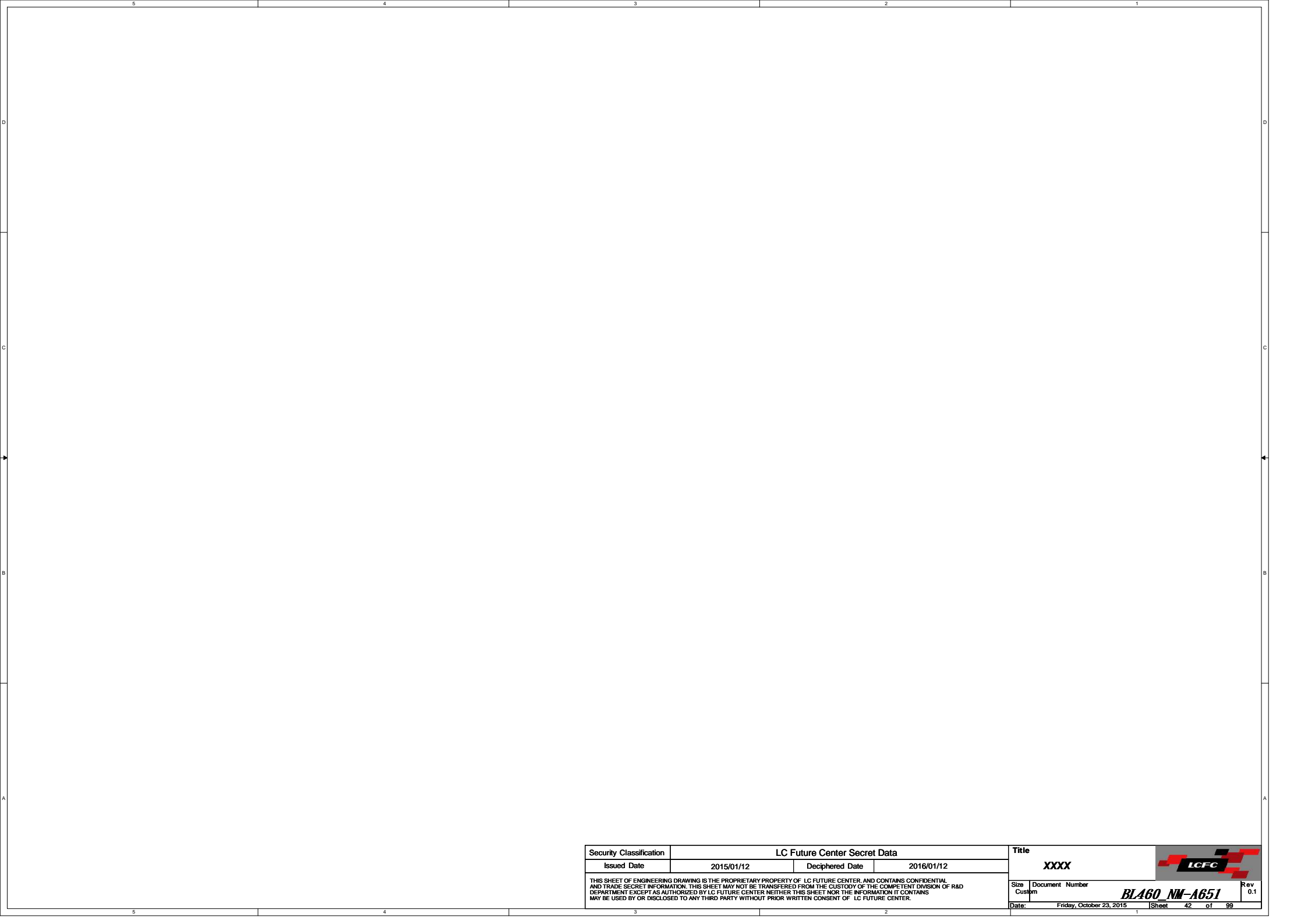
Nominal at 0.95 V, can support up to 1.05 V functionally.


PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	STRAP_BIOS_ROM_EN = 1 ROM_CONFIG[2:0] = [001] 256MB
PS_0[4]	N/A	1 (Default)
PS_0[5]	N/A	1 (Default)
PS_1[1]	STRAP_BIF_GEN3_EN_A	0 = PCIe GEN3 is not supported
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled
PS_1[3]	N/A	0 (Default)
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	1 = The transmitter full-swing is enabled
PS_1[5]	STRAP_TX_DEEMPH_EN	1 = Tx deemphasis enabled
PS_2[1]	N/A	0 (Default)
PS_2[2]	N/A	0 (Default)
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device
PS_2[4]	N/A	1 (Default)
PS_2[5]	N/A	1 (Default)
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	PS_3[3..1] 101 = Micron 2G 110 = Samsung 2G 111 = Hynix 2G
PS_3[4]	N/A	1 (Default)
PS_3[5]	N/A	1 (Default)

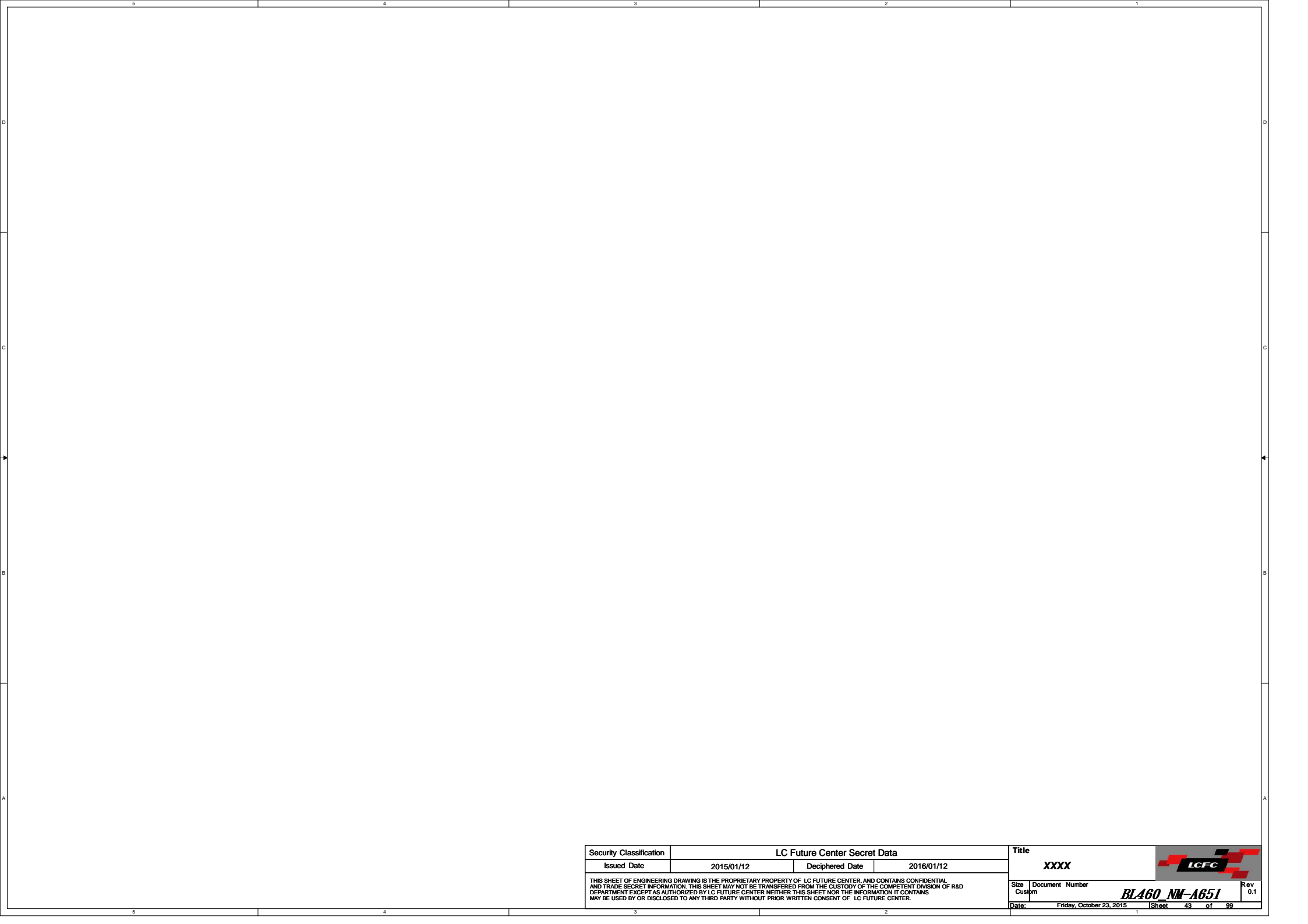
Security Classification		LC Future Secret Secret Data		Title			Rev. 0.
Issued Date	2015/01/12	Deciphered Date	2016/01/12	XXXX			
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				Date:	Friday, October 23, 2015	Sheet 40 of 99	




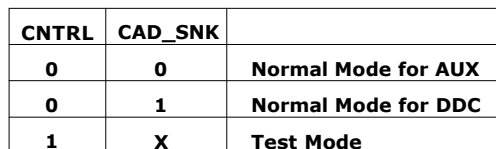
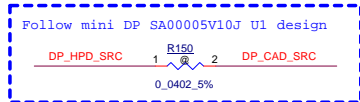
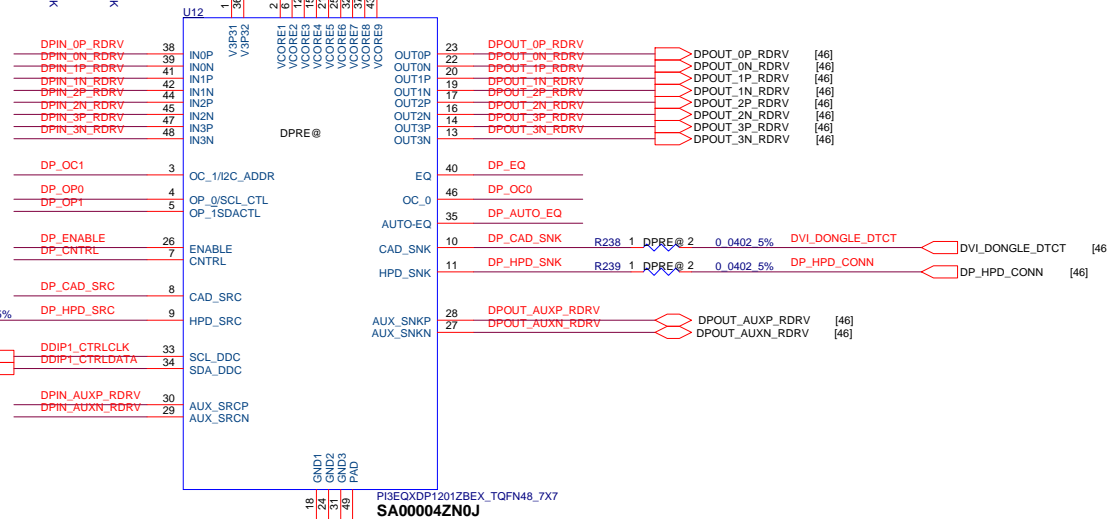
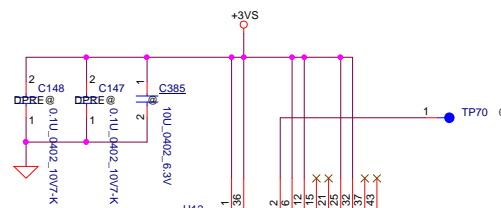
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Issued Date		2015/01/12	Deciphered Date	2016/01/12	XXXX		
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Date:					Friday, October 23, 2015	Sheet	41 of 99

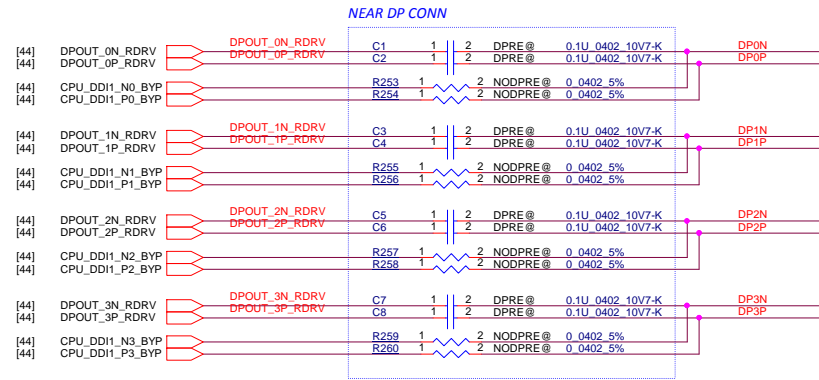


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				Custom			
				Date:	Friday, October 23, 2015	1	Sheet 42 of 99



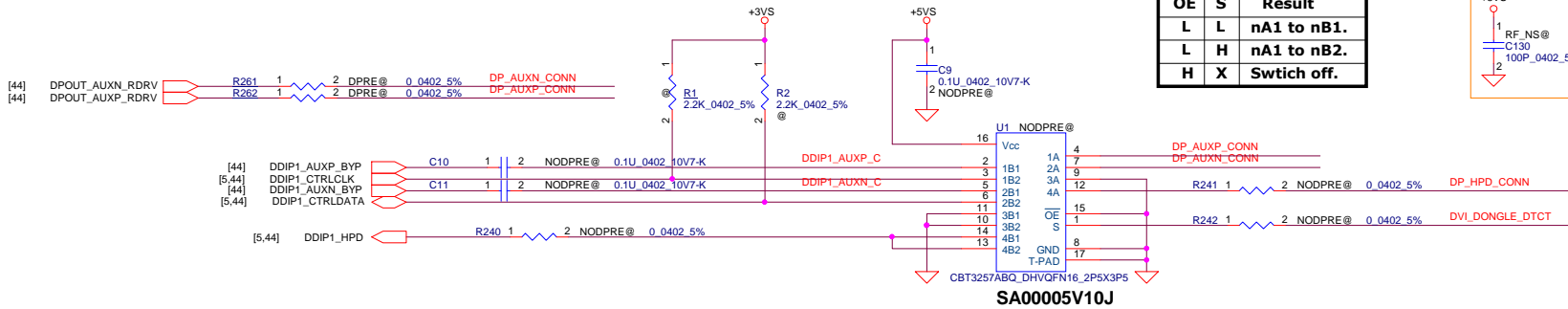
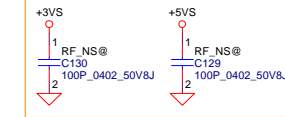
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Issued Date	2015/01/12	Deciphered Date	2016/01/12	XXXX			
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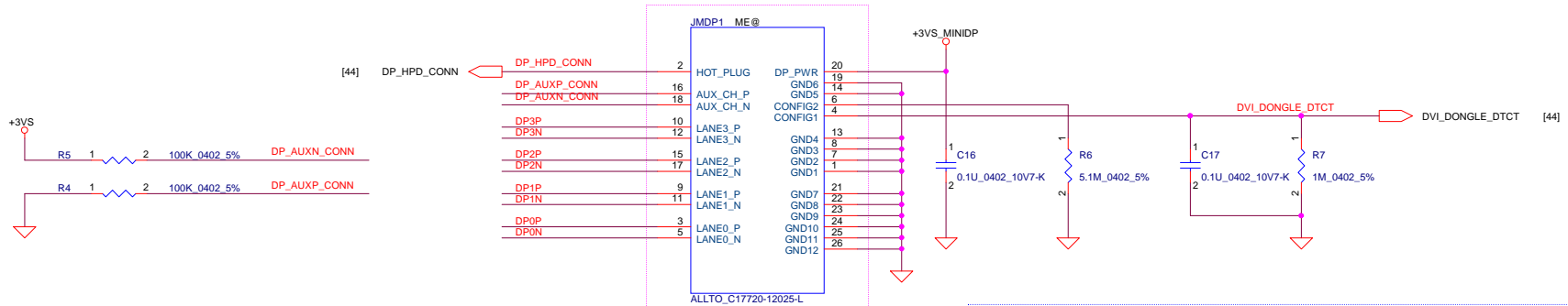


OE	S	Result
L	L	nA1 to nB1.
L	H	nA1 to nB2.
H	X	Switch off.

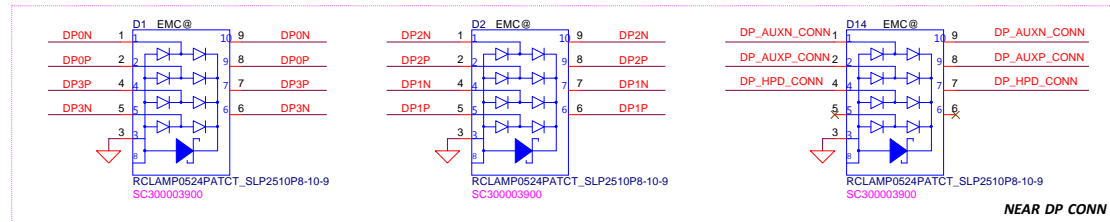
Reserve capacitor for LTE noise 2014.5.21



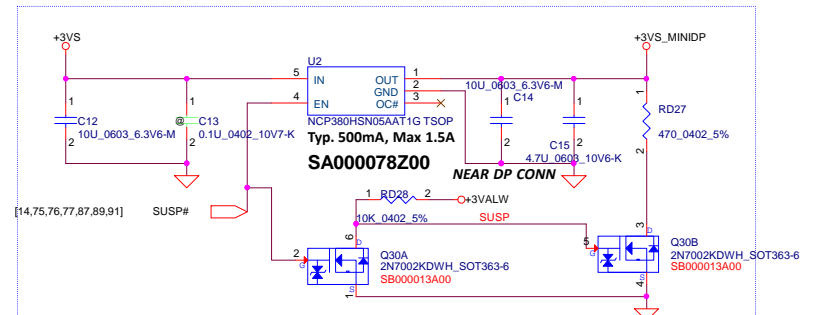
SA00005V10J




EMC (ESD soluti on)

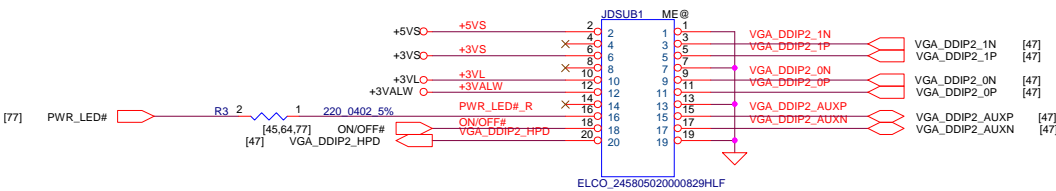


NEAR DP CONN

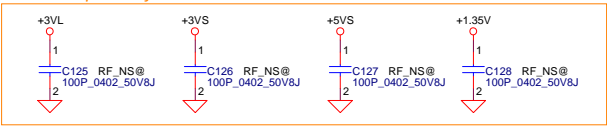


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						Rev	0.1


M/B TO D-SUB/B BTB CONN.

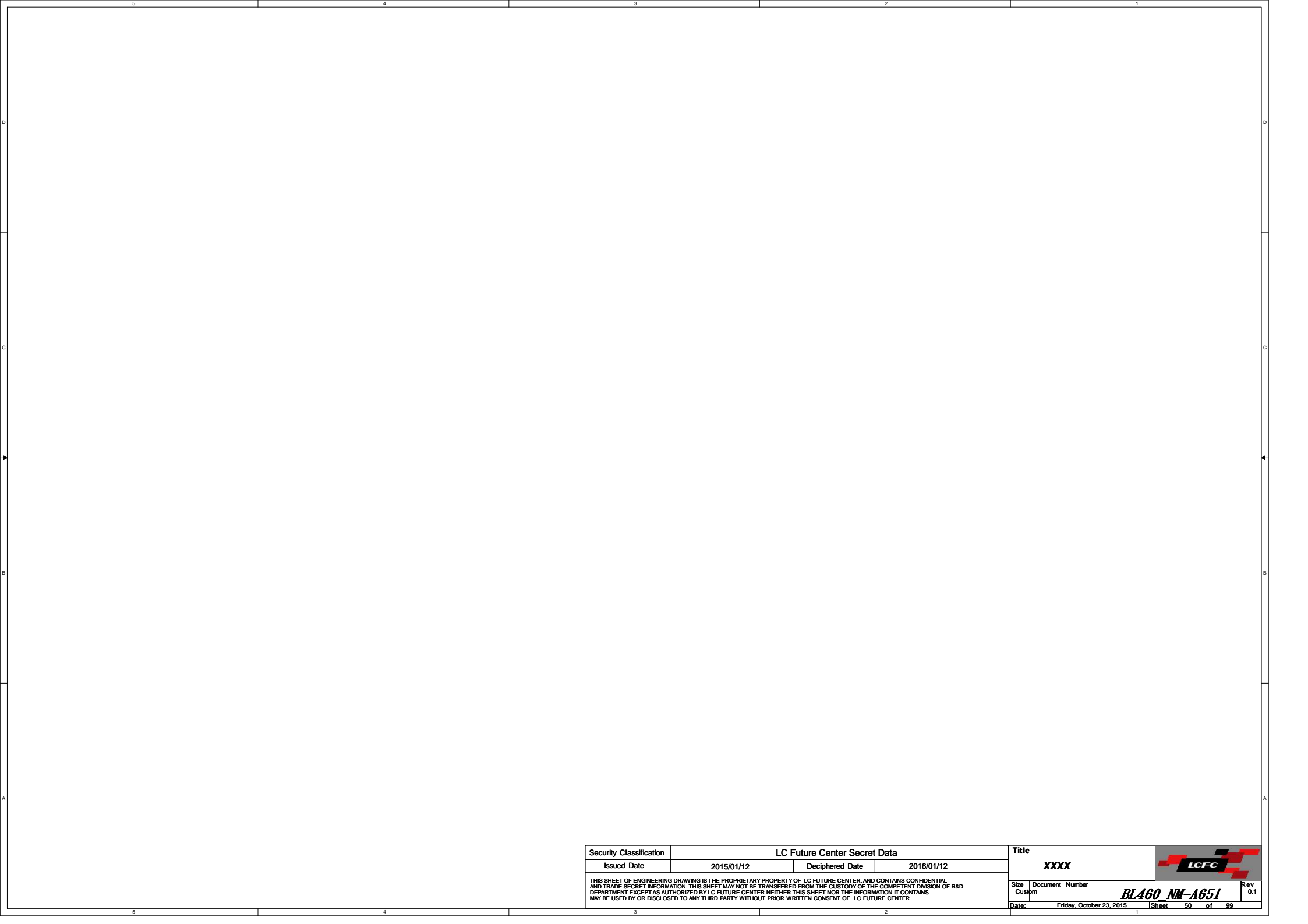



Reserve capacitor for LTE noise 2014.5.21



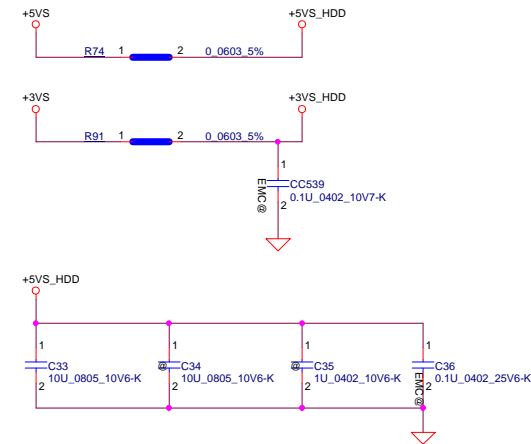
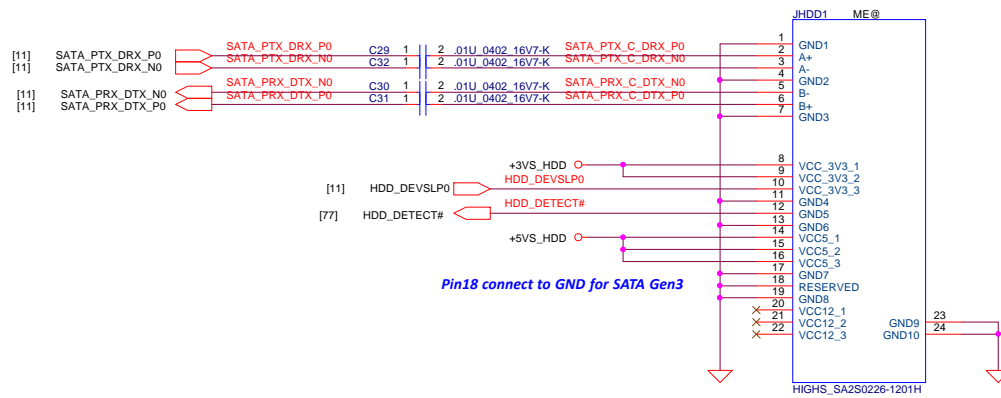
	A	B	C	D	E
1					
2					
3					
4					

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Issued Date	2015/01/12	Deciphered Date	2016/01/12		XXXX		
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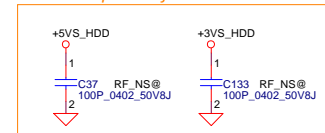




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				Custom			
				Date:	Friday, October 23, 2015	Sheet	50 of 99

SATA HDD CONN.

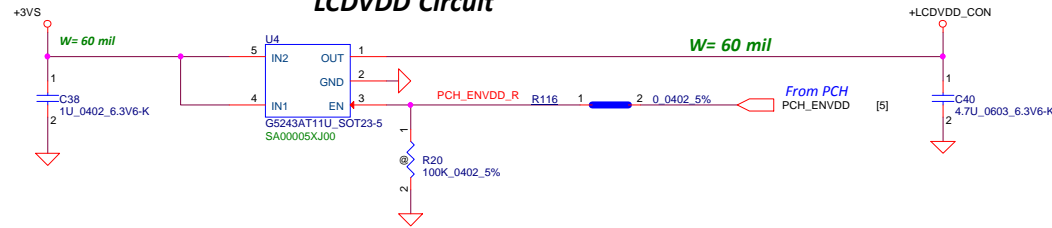


Reserve capacitor for LTE noise 2014.5.21

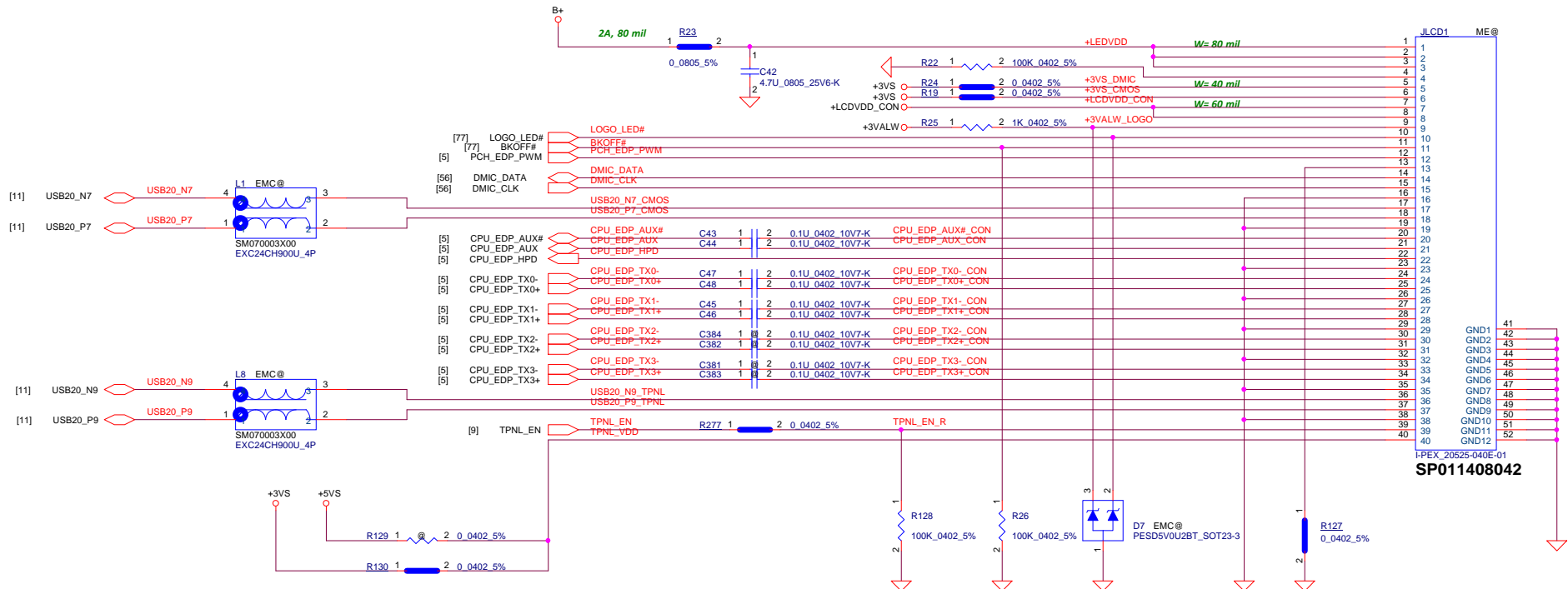


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Issued Date	2015/01/12	Deciphered Date	2016/01/12	SATA HDD CONN.		
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Date:		Friday, October 23, 2015		Sheet 51 of 99		

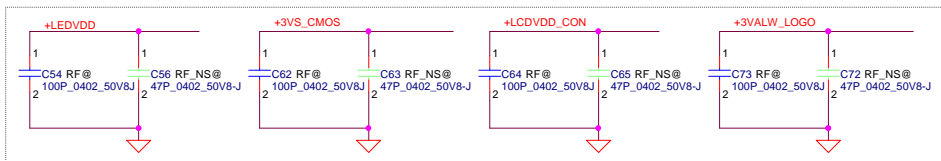
LCDVDD Circuit



eDP/CMOS/LOGO-LED CONN.



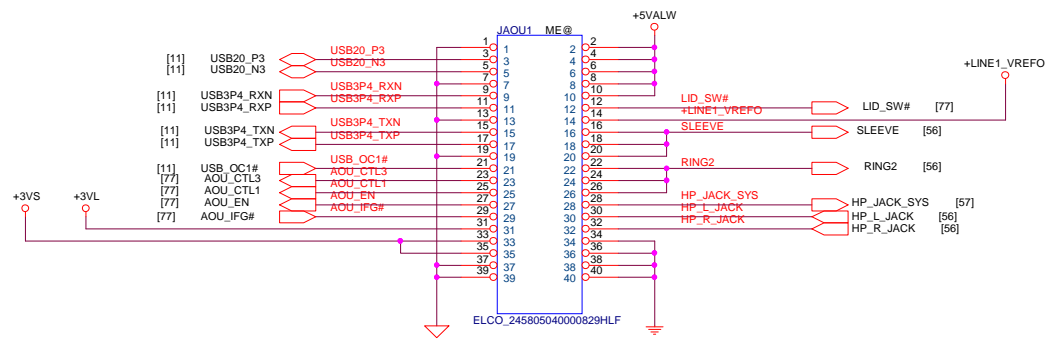
RF




LC Future Center Secret Data			
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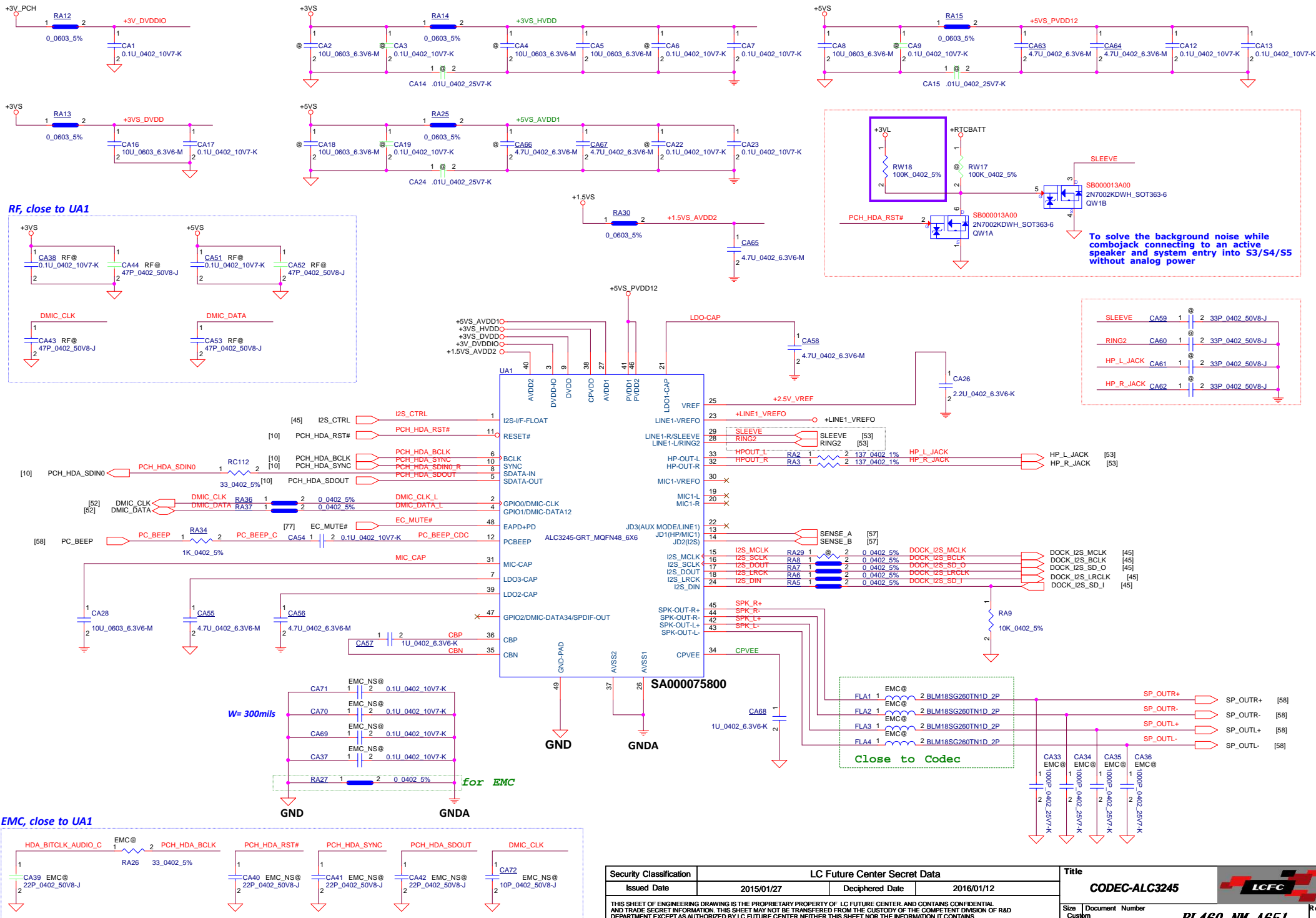
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Size	Document	Number	Rev
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Date:	Friday, October 23, 2015		
	Sheet	52	of 99

AOU/JACK/LID-SW BTB CONN.

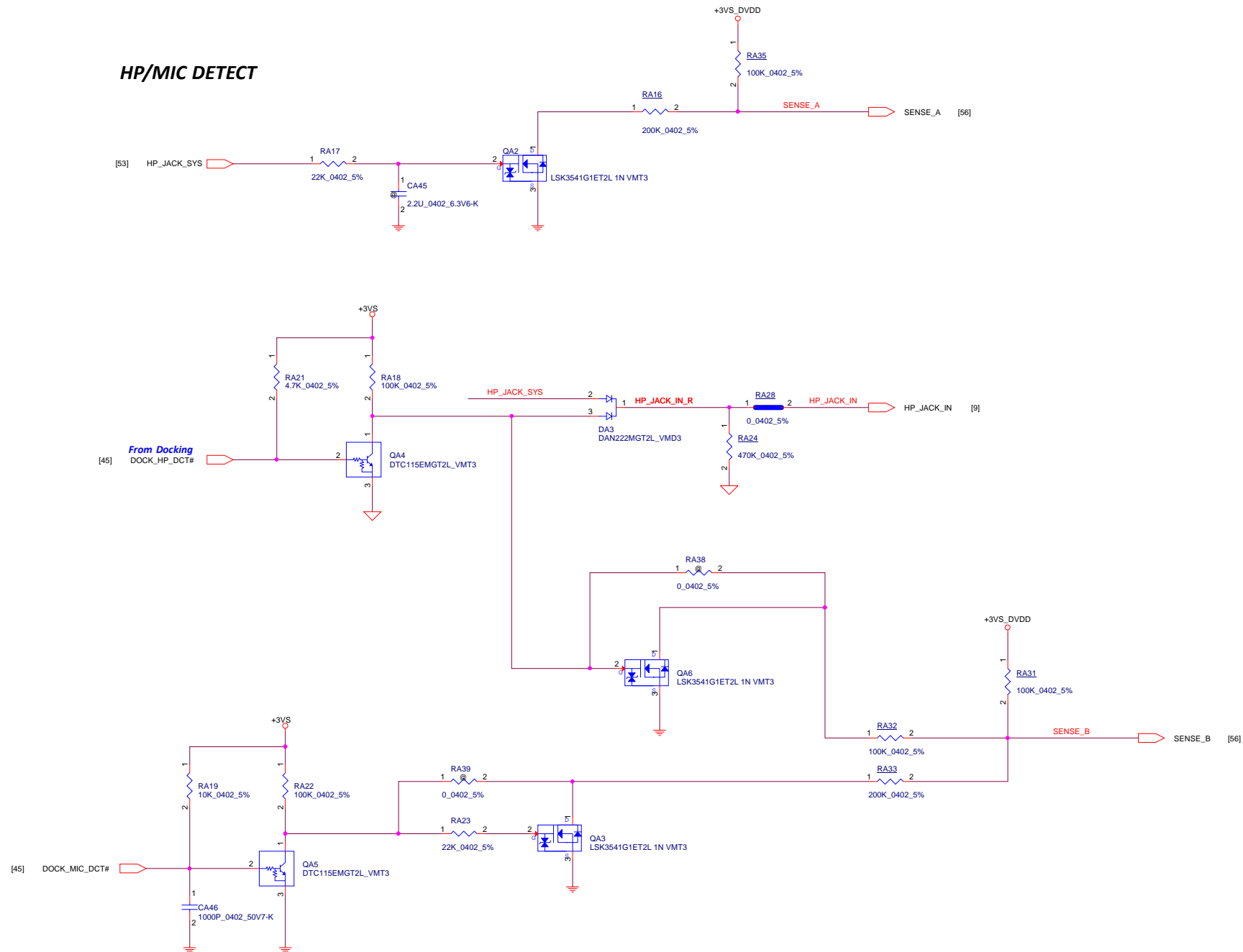



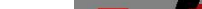
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D					
C					
B					
A					

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Date:		Friday, October 23, 2015		4:41 PM		Sheet		55 of 99	



HP/MIC DETECT



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Issued Date	2015/01/12	Deciphered Date	2016/01/12	HP/MIC DETECT		
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				Date: Friday, October 23, 2015 Sheet 57 of 99		


SP_OUTL+
SP_OUTL-
SP_OUTR-
SP_OUTR+

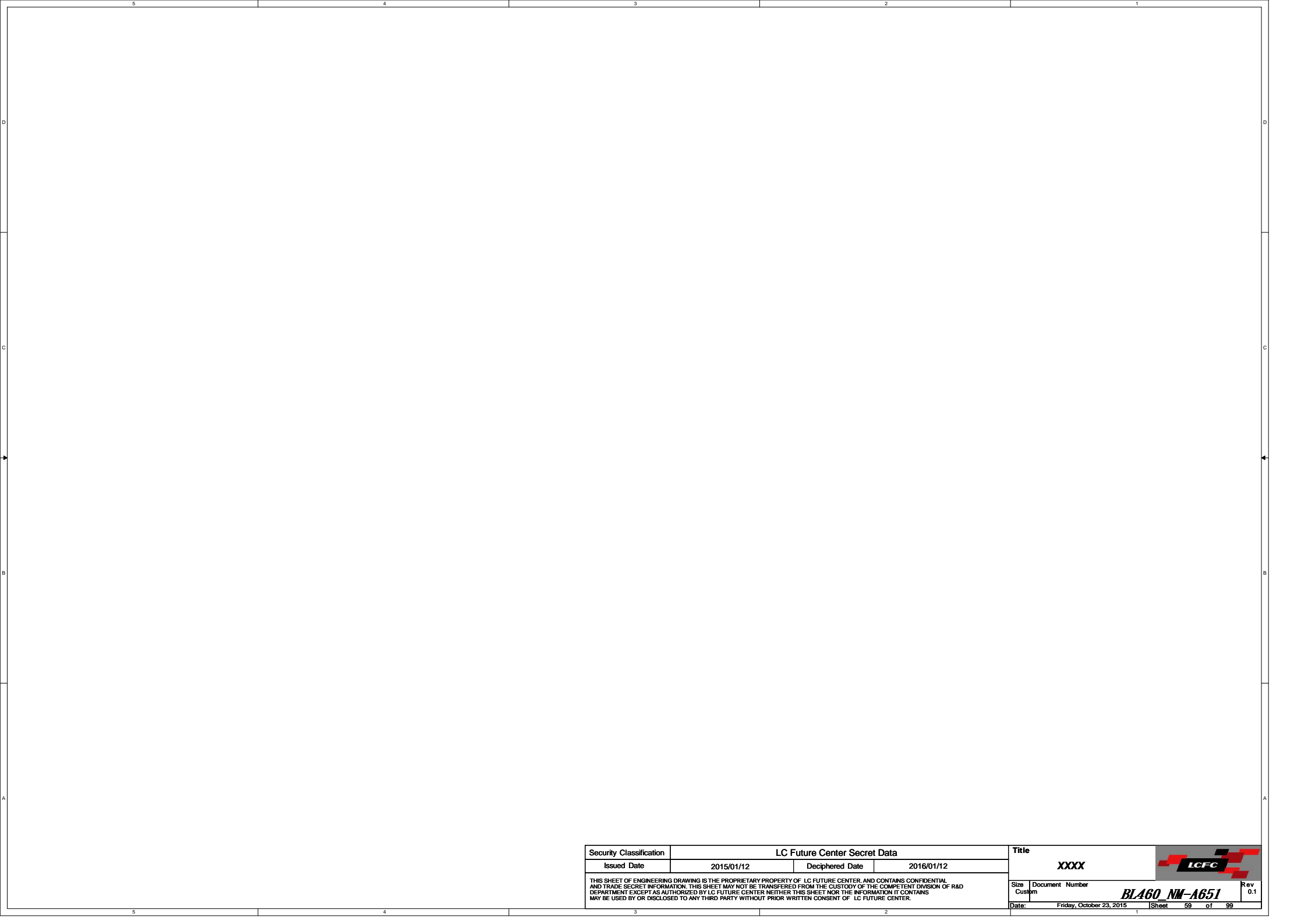
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CA48 EMC_NS@ 220P_0402_50V7-K
CA49 EMC_NS@ 220P_0402_50V7-K
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JSPK1 ME@
1
2
3
4
5
6
GND1
GND2

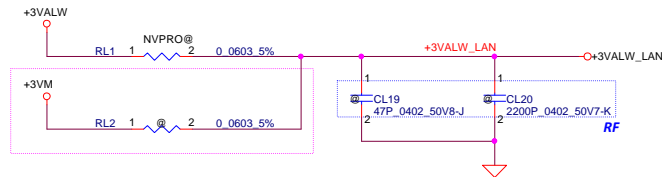
SP011212121

Close to SPEAKER CONN.

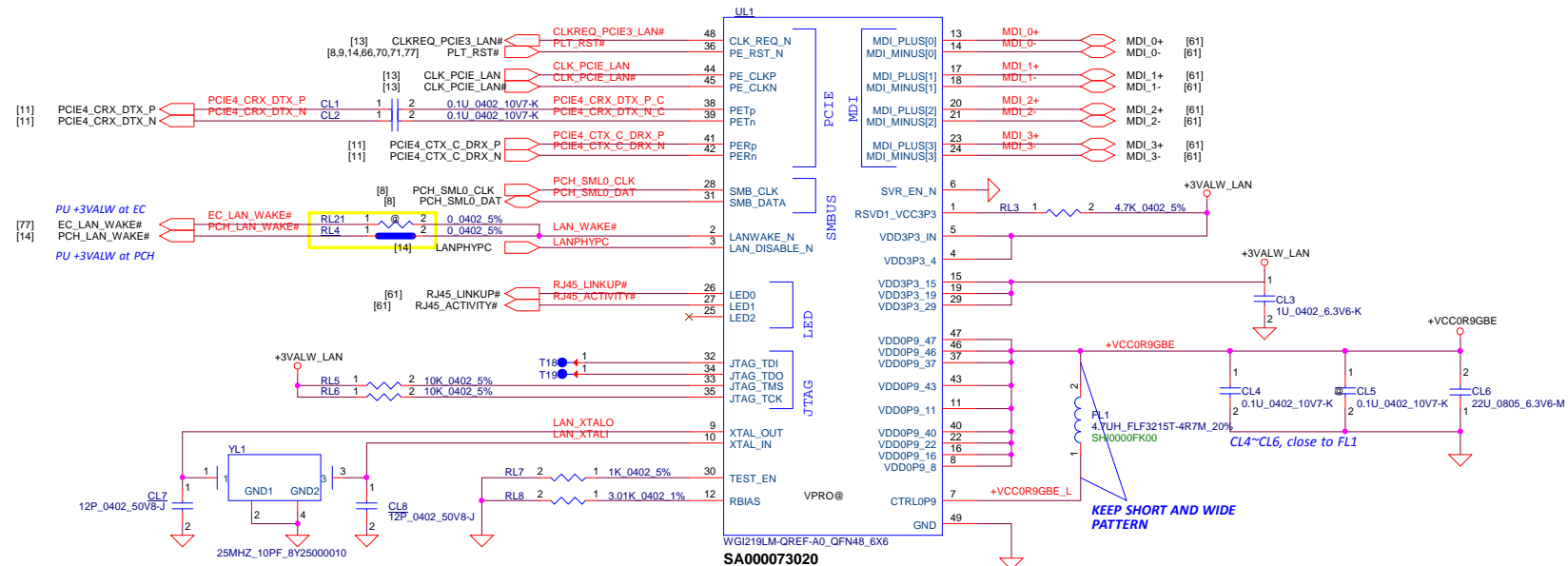
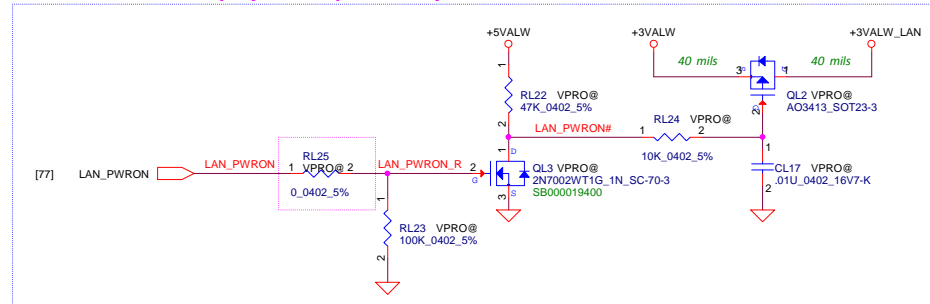
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Issued Date	2015/01/12	Deciphered Date	2016/01/12	PCBEEP/SPK CONN.			
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						Rev 0.1	



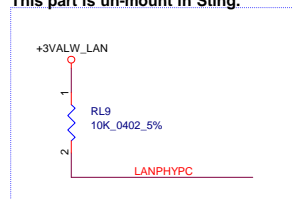
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Custom				BL460_NW-A651		0.1			
Date:		Friday, October 23, 2015		Sheet		59 of 99			



VPRO SKU : RL2 (@), RL25(VPRO@)

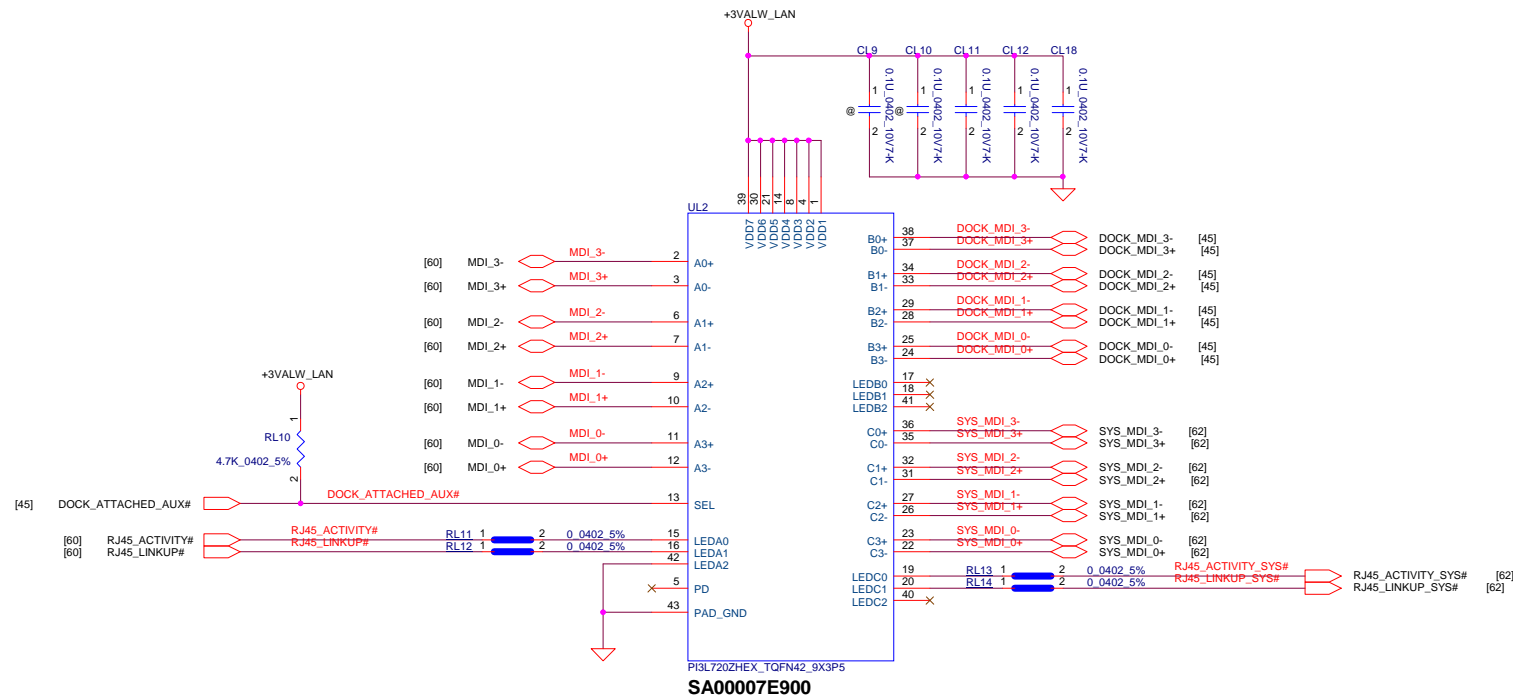


When use Native function, intel recommend pull high 10K ohm.
This part is un-mount in Sting.



UL1 GBE PHY

	Model	P/N
vPro	WGI219LM	SA000073020
non-vPro	WGI219V	SA000072Z00



Vendor	P/N	NOTE
Pericom	PI3L720ZHE+CX, SA00007E900	Main Source
ONsemi	NCN7201 , SA00005TF00	2nd Source (FVT)

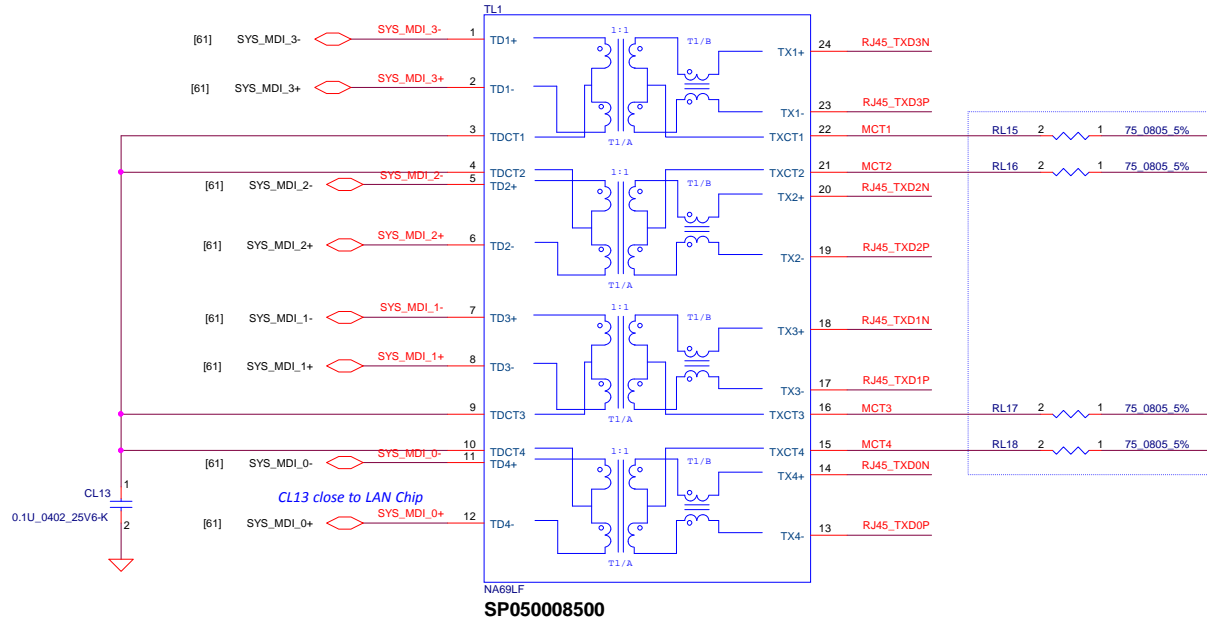
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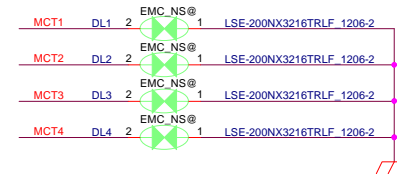
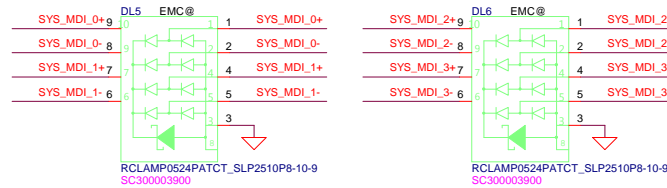
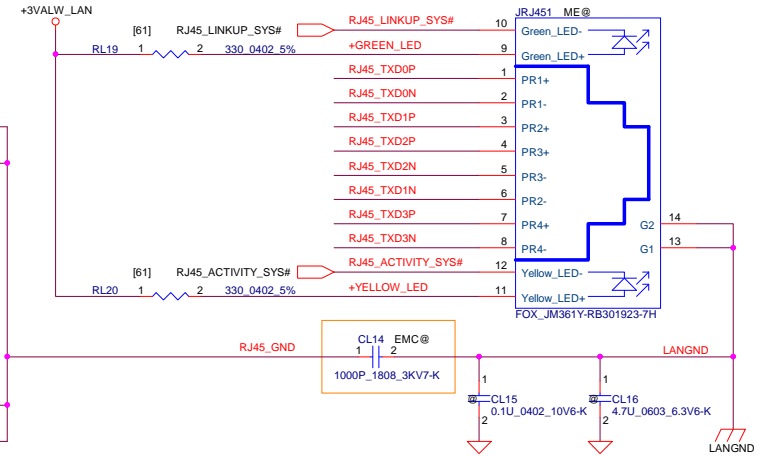
BL460_NW-A651

Rev 0.1

LAN X' FORM

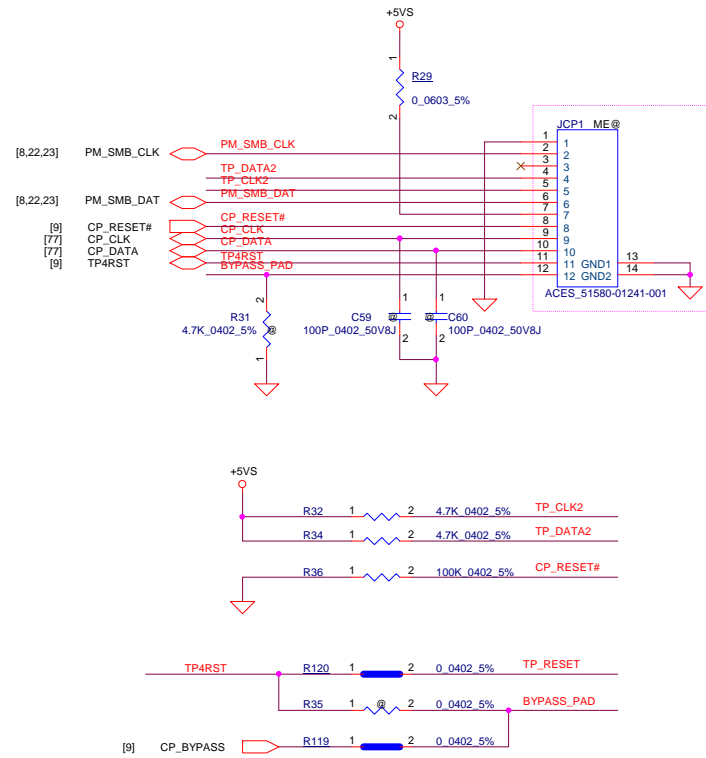


RJ45 Conn.

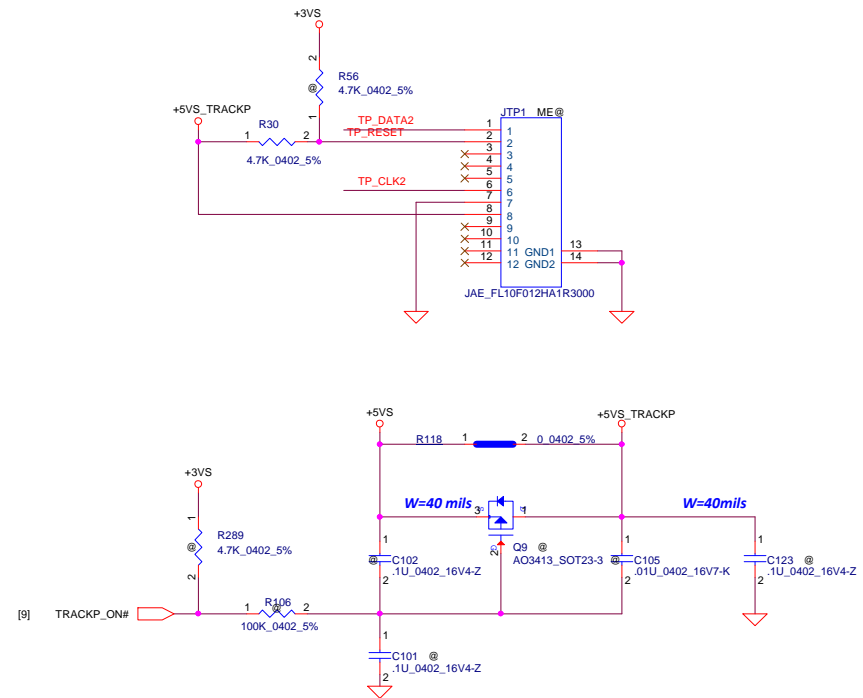


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Date:				Friday, October 23, 2015		Sheet		62 of 99			

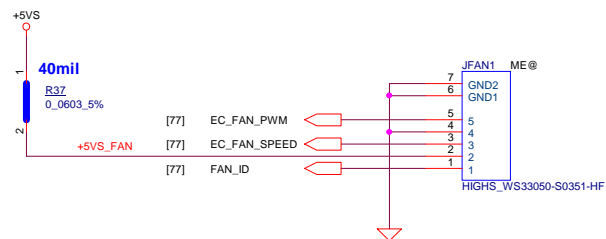
5-Button Click Pad



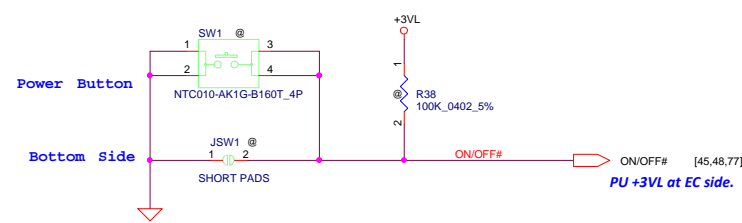
Track Point

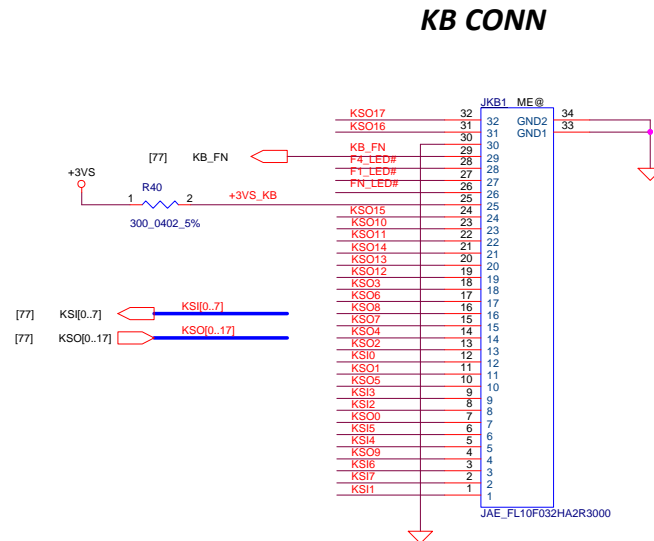
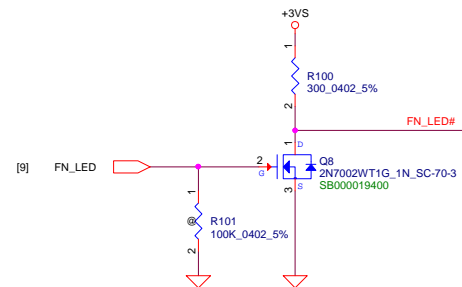
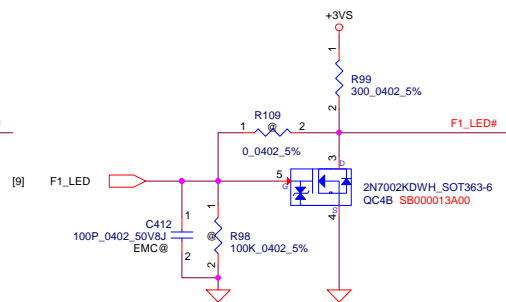
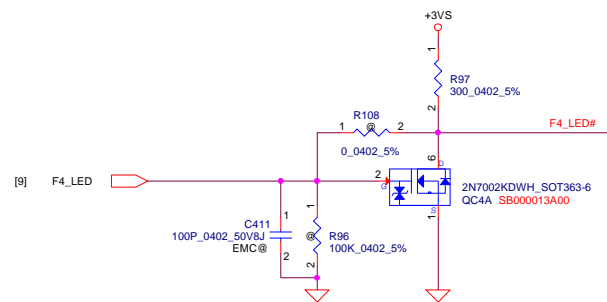


FAN CONN.

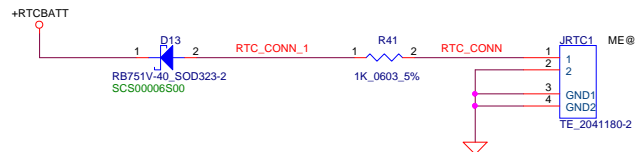


PWRBTN FOR DENUG

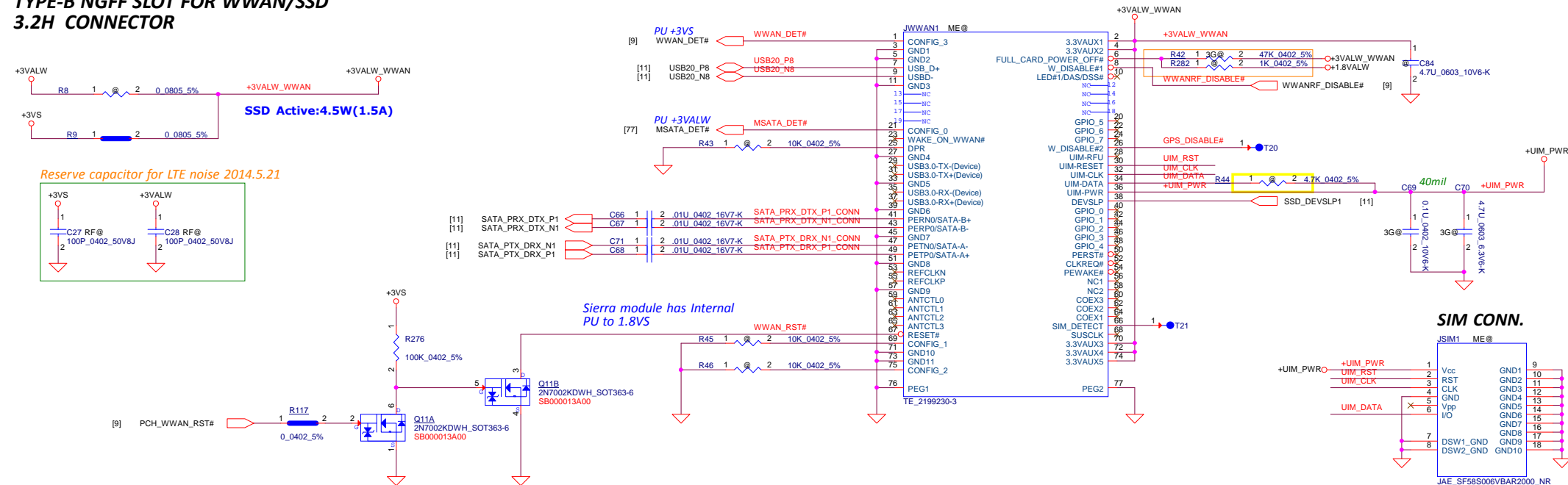




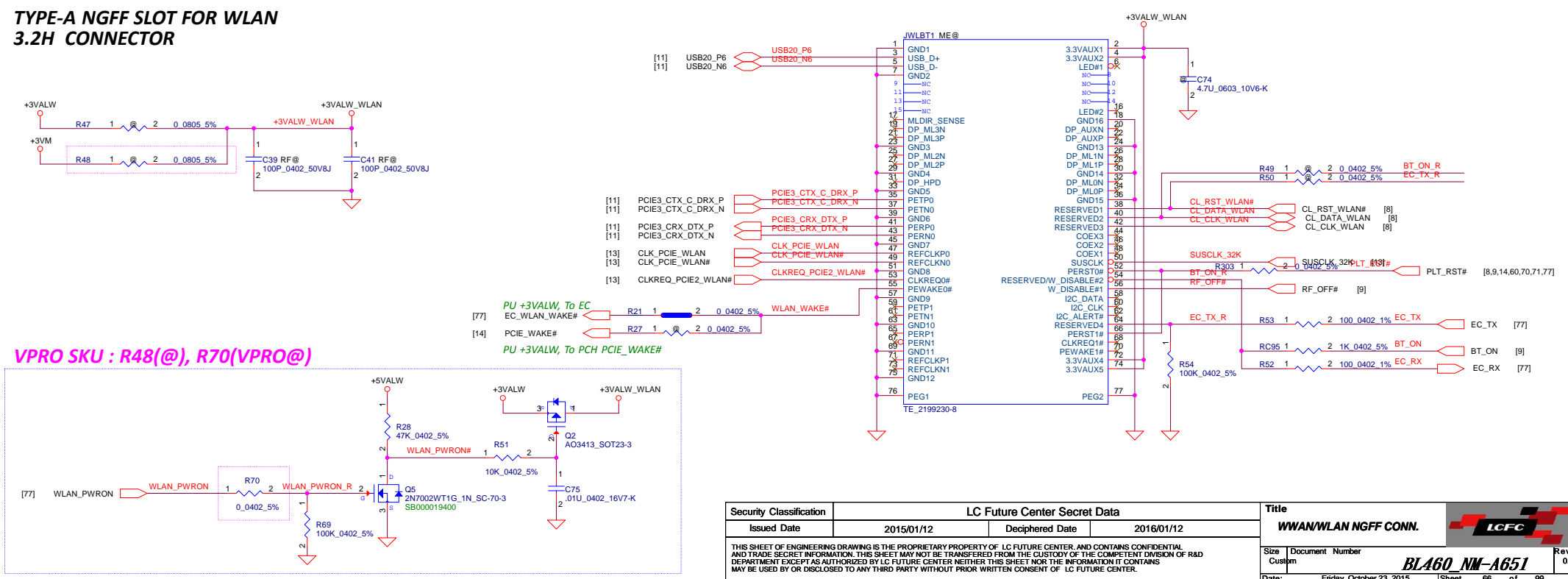
RTC CONN.

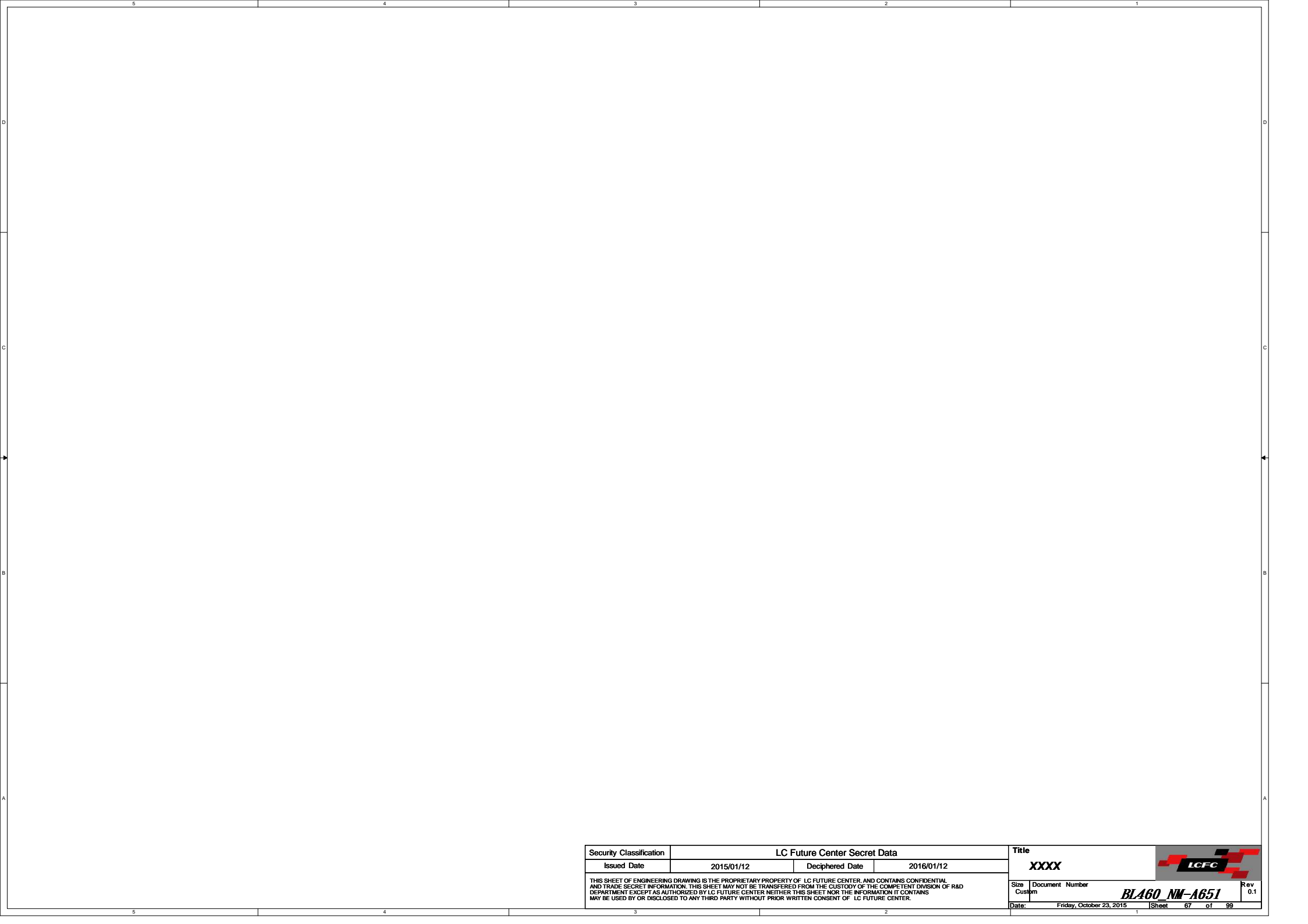



TYPE-B NGFF SLOT FOR WWAN/SSD 3.2H CONNECTOR

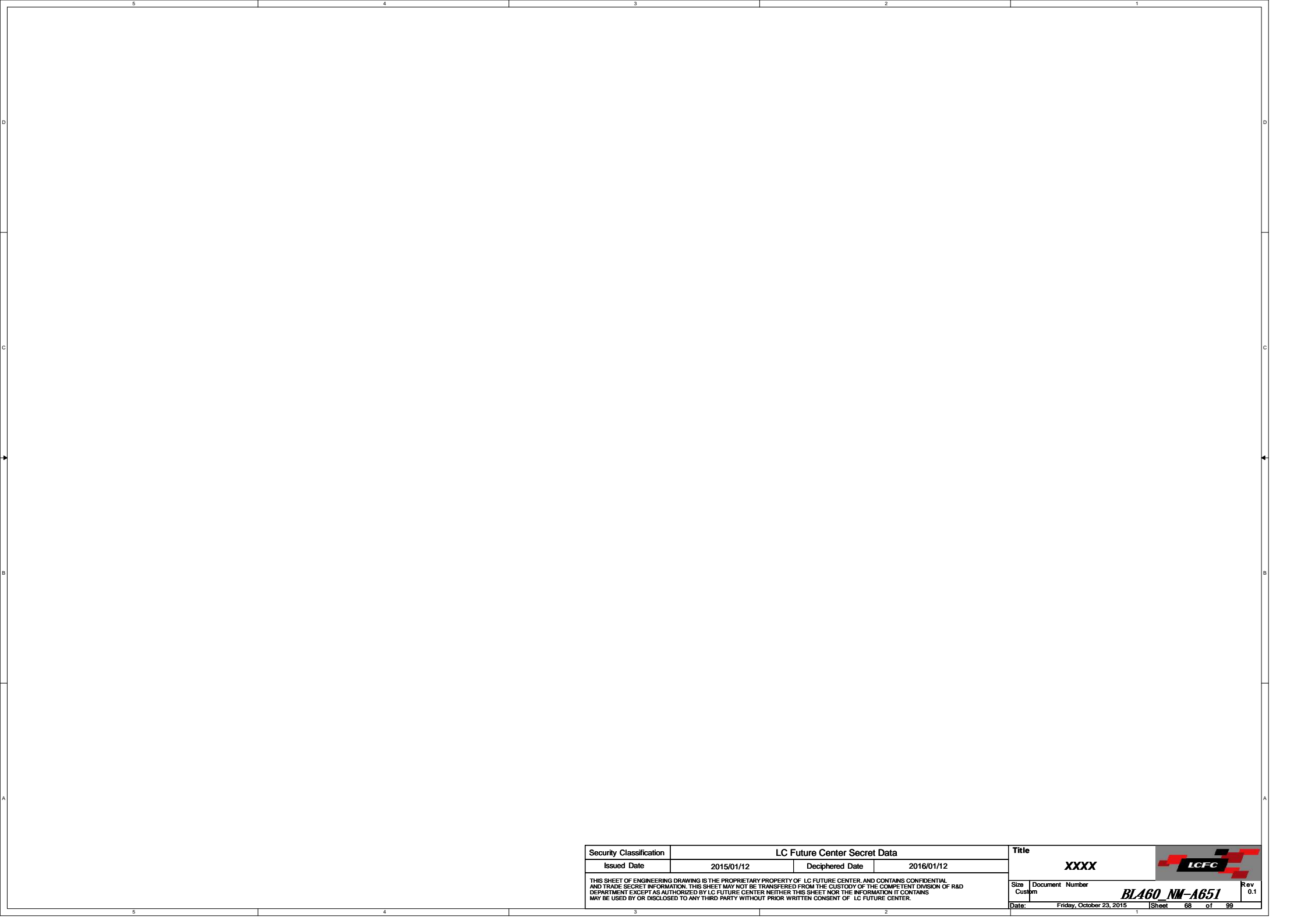



TYPE-A NGFF SLOT FOR WLAN 3.2H CONNECTOR



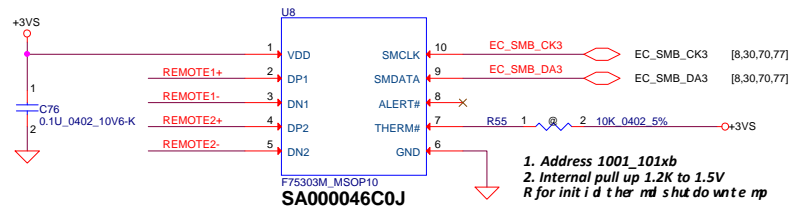


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				Custom	BL460_NW-A651	0.1	
Date:				Friday, October 23, 2015 1 Sheet 67 of 99			

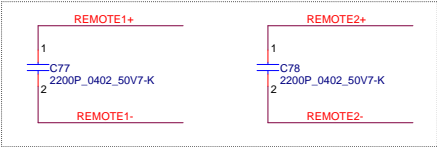


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Issued Date	2015/01/12	Deciphered Date	2016/01/12	XXXX		
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				Date:	Friday, October 23, 2015	Rev 0.1
				Sheet 68 of 99		

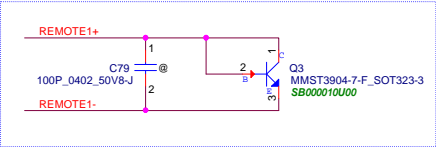
Thermal Sensor



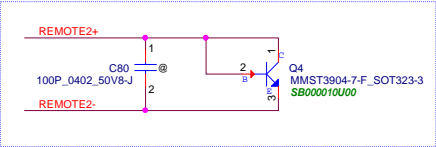
Close to U8



Close to +VCC_CORE

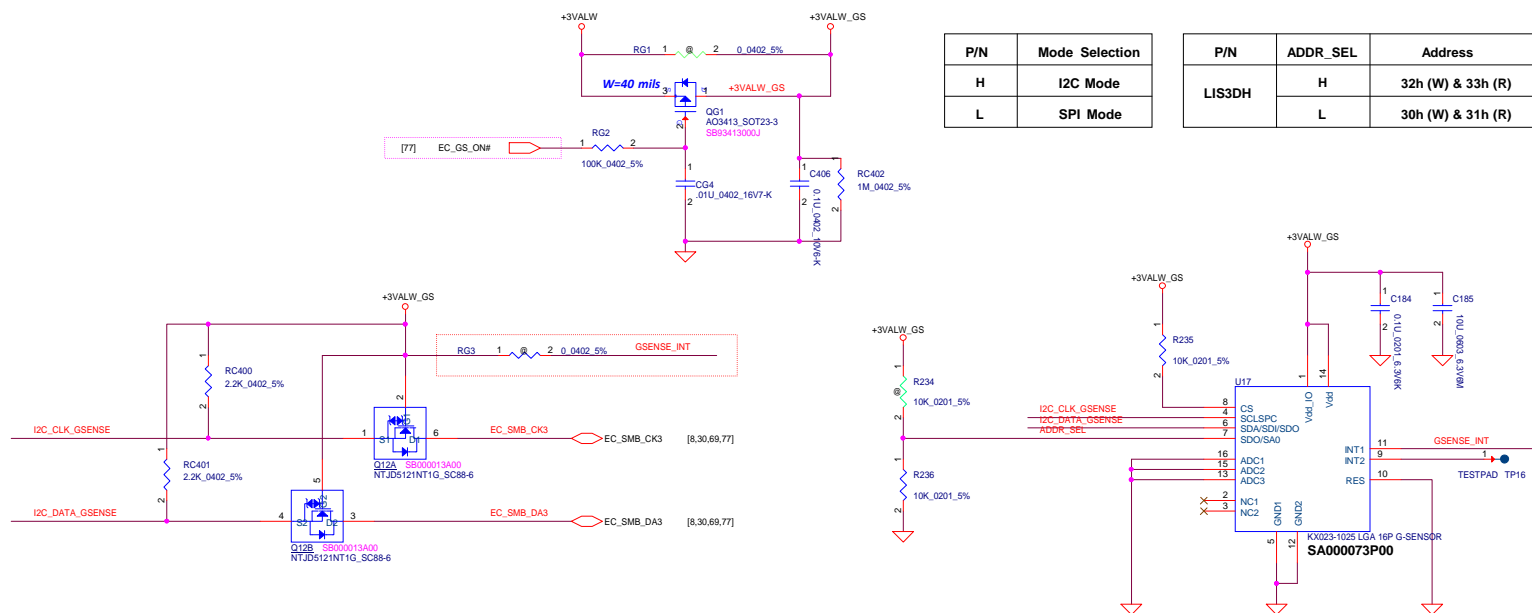
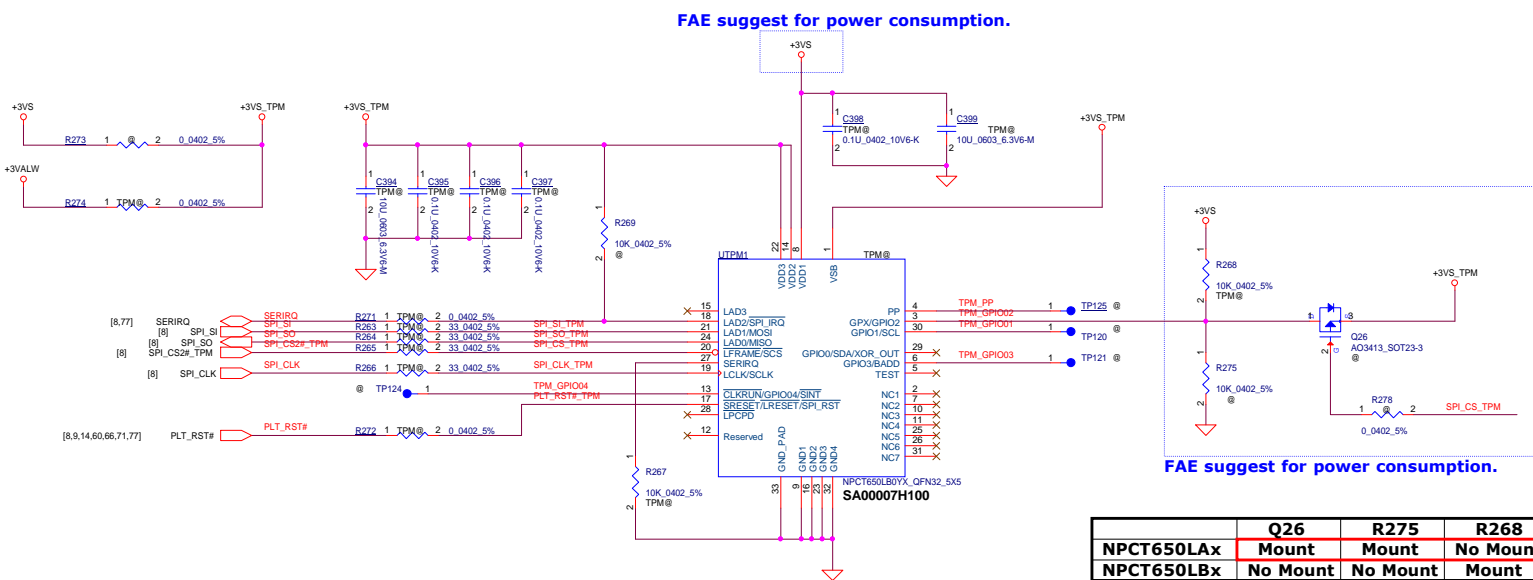


Close JDIMM1&JDIMM2

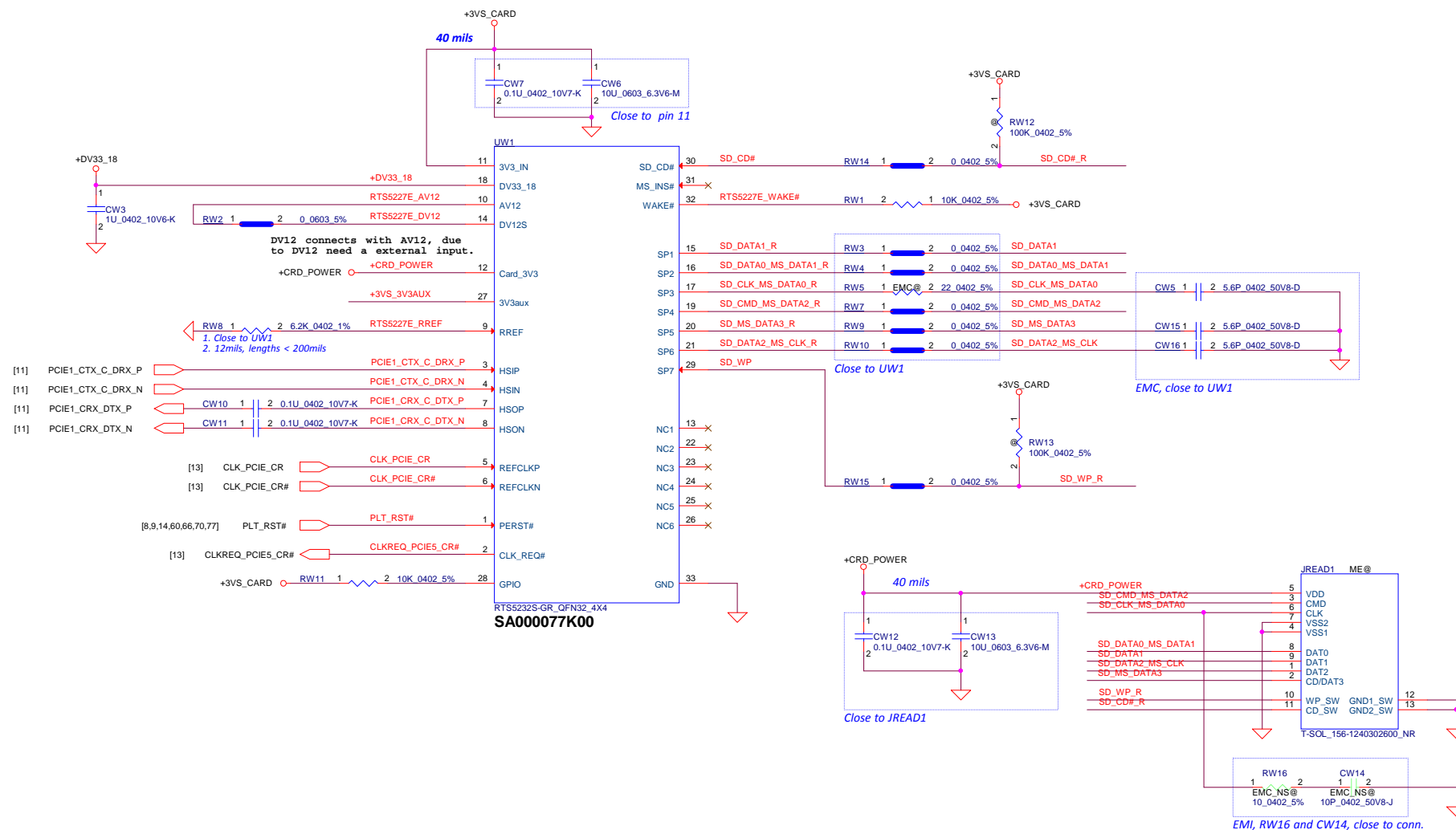
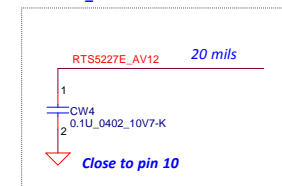
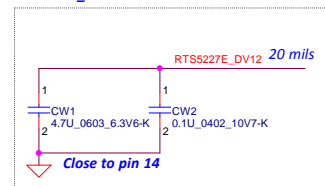
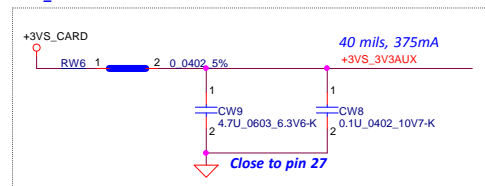
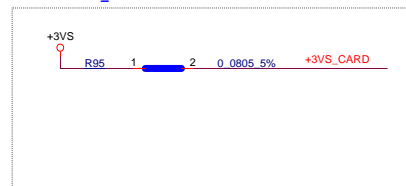


REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"


APS G-Sensor

**TPM IC**

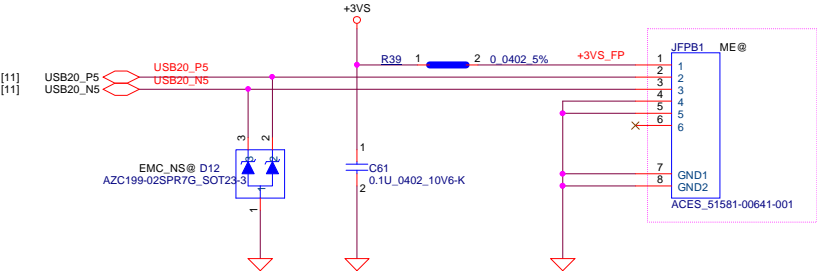
	Q26	R275	R268
NPCT650LAx	Mount	Mount	No Mount
NPCT650LBx	No Mount	No Mount	Mount



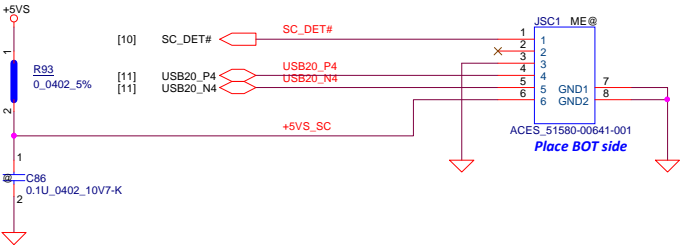
Connector side / IC side	WP		CD
	Lock	Unlock	
Card insertion	L	H	H
Card uninserction	L	L	L


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FingerPrint CONN.

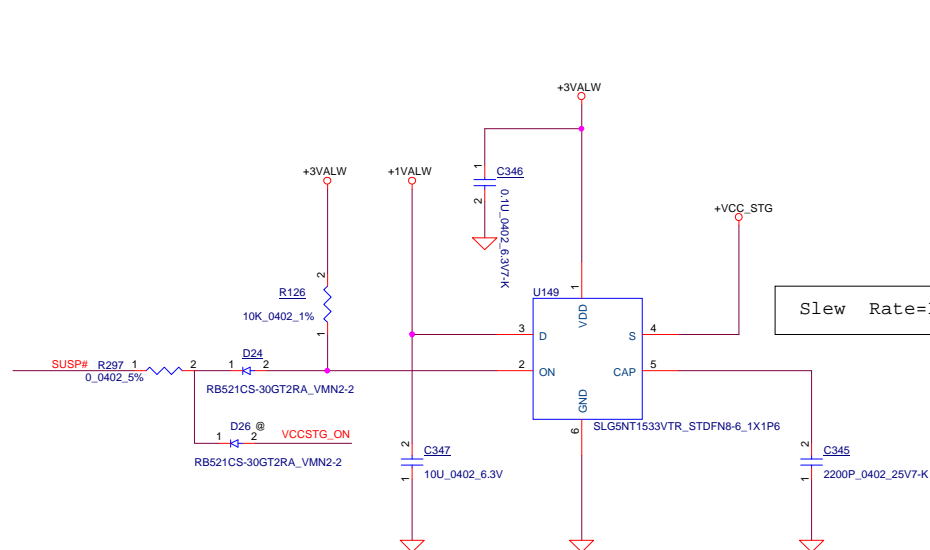
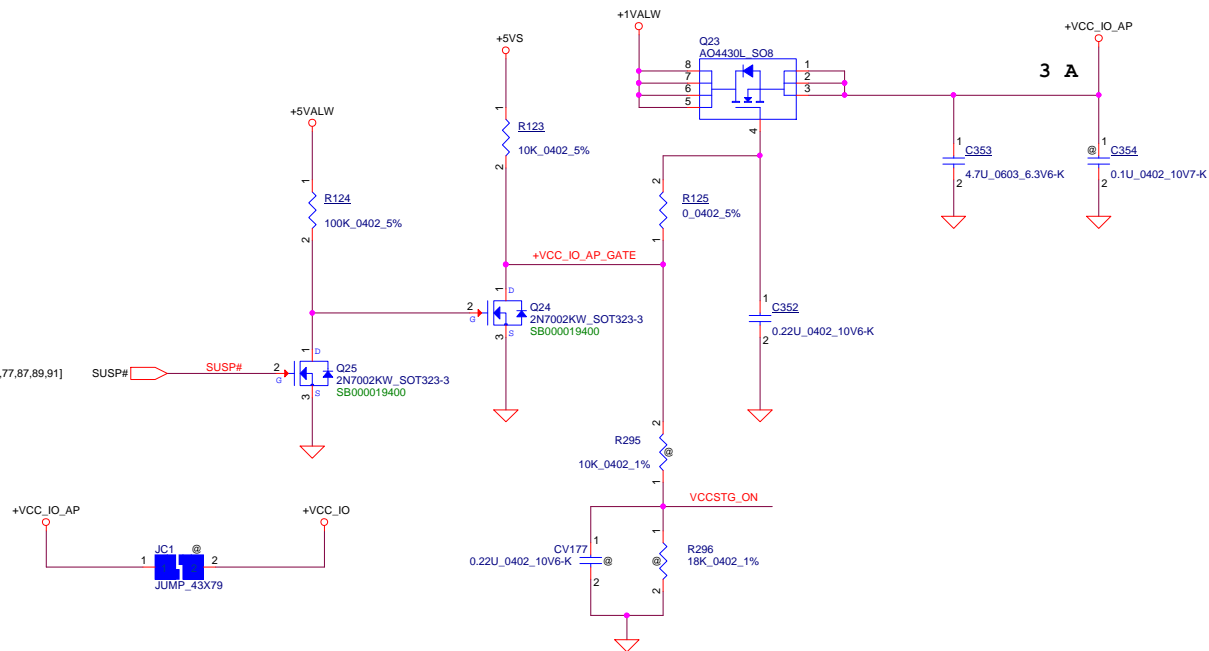


SMART CARD CONN.

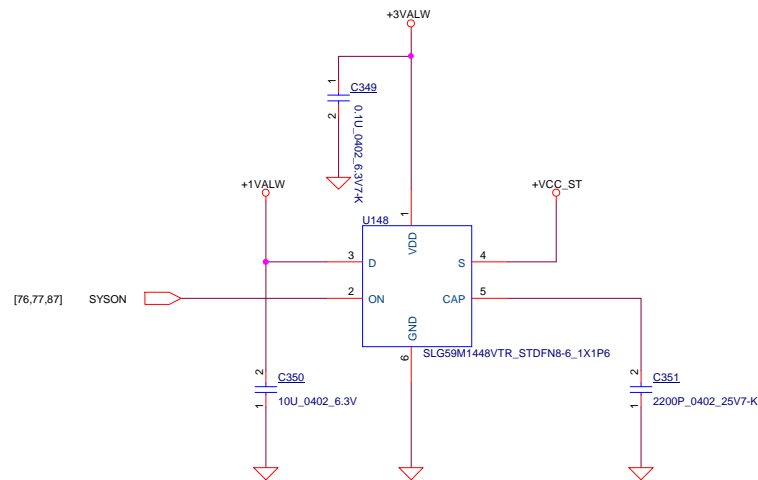


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Issued Date	2015/01/12	Deciphered Date	2016/01/12	XXXX		
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				Date: Friday, October 23, 2015 Sheet 74 of 99		Rev 0.1

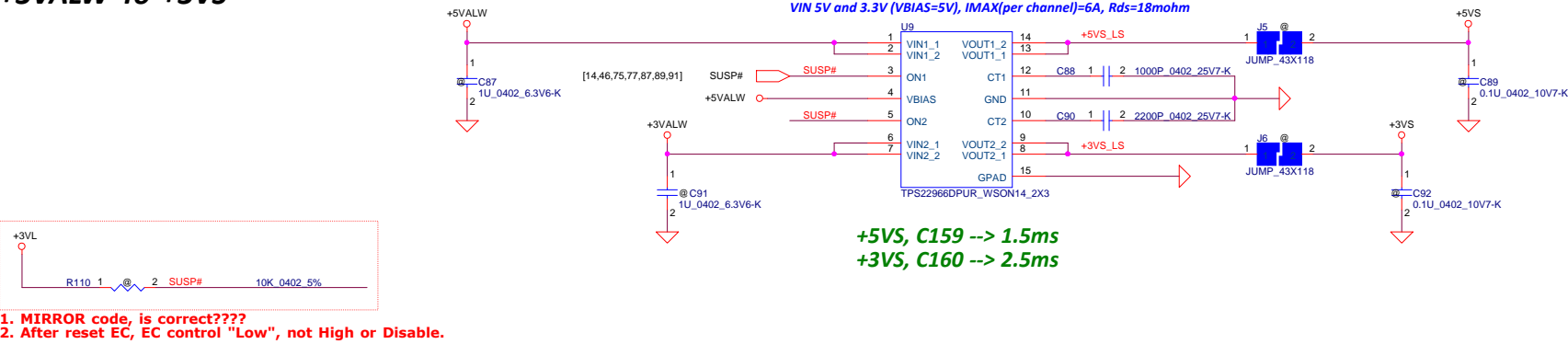
+1VALW to +VCC_IO_AP



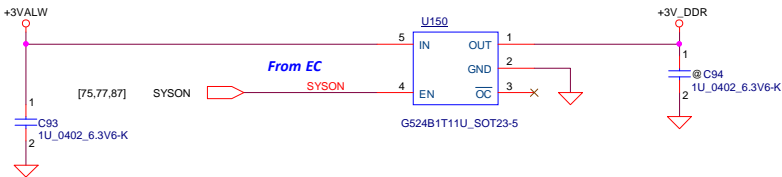
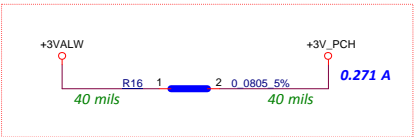
Slew Rate=10uS<TR<65us



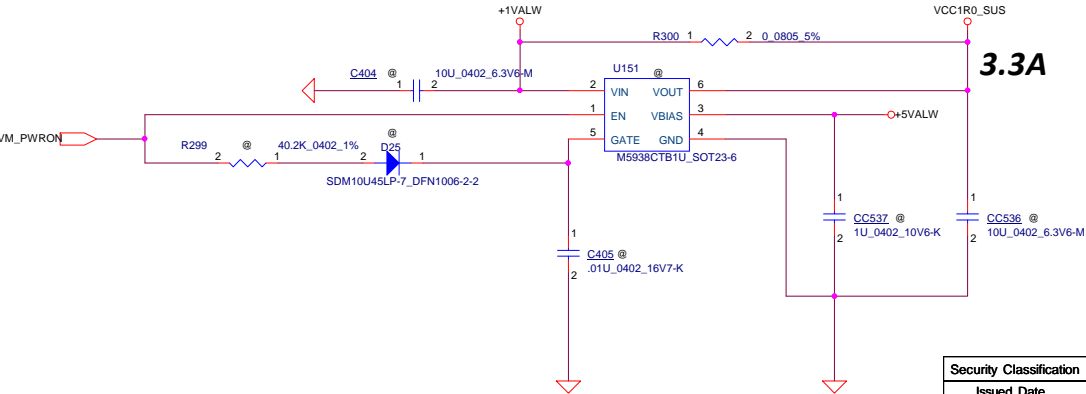
Smart Switch
+5VALW To +5VS
+3VALW To +3VS



+3VALW To +3V_PCH : Short, Don't support Deep Sx

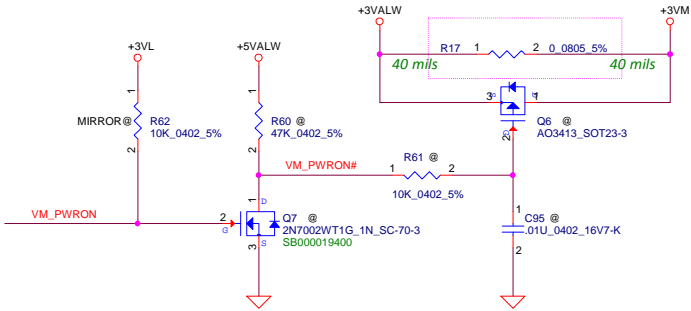


+1VALW to VCC1R0_SUS

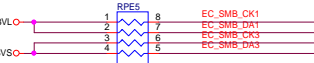
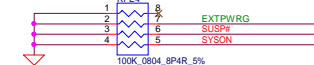
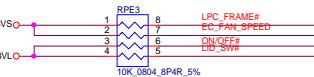
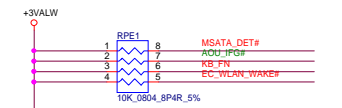
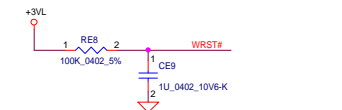
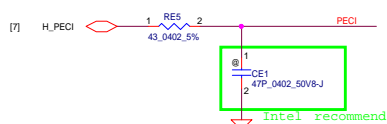


+3VALW to +3VM
VPRO : SPI ROM

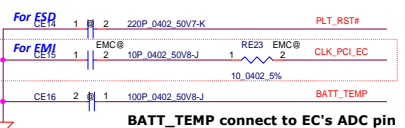
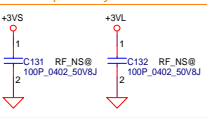
+3VM to SPI ROM.
Reserve for LAN and WLAN.



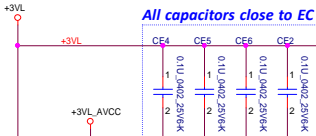
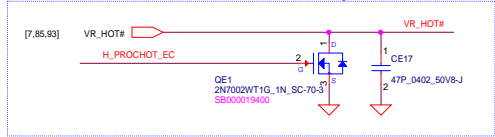
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Issued Date	2015/01/12	Deciphered Date	2016/01/12	Size		
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Reserve capacitor for LTE noise



PROCHOT#
(EC asserts PROCHOT# signal by driving high, the level shifter must invert it and drive the processor side PROCHOT# low.)



minimum trace width 12 mil

**IT8586E/AX
LQFP-128L**

Int. K/B Matrix

EXTERNAL SERIAL FLASH

SPI Flash ROM

UART

SM Bus

GPIO

WAKE UP

GPIO

Clock

EC_AGND

IT8586E/AX LQFP128, 14X14

SA00005W940

EC_AGND

EC_AGND

EC_AGND

EC_AGND

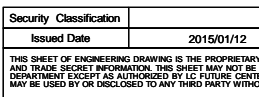
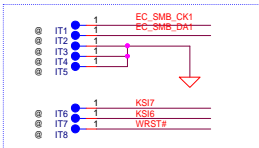
EC_AGND

EC_AGND

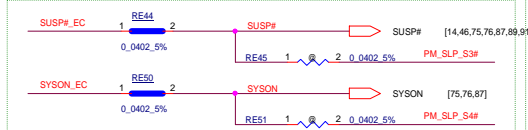
EC_AGND

Please don't place any PU Resistor on GPG1[7:2]
(Reserve hardware strapping)

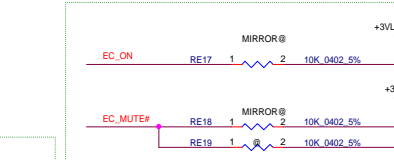
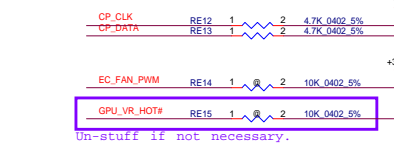
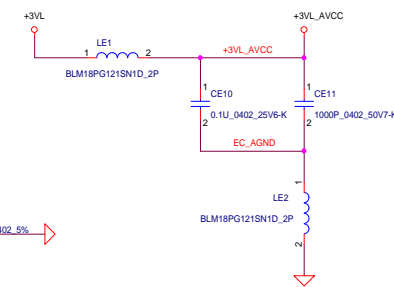
For factory EC flash



Reserved for HW control

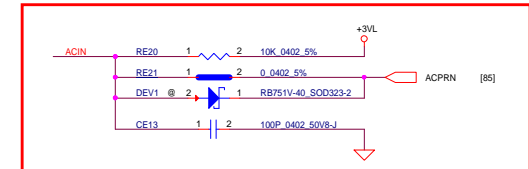


Vcc	3.3V +/- 5%
RE6	100K +/- 1%
Board ID	RE7
0	0K +/- 5%
1	8.2K +/- 5%
2	18K +/- 5%
3	33K +/- 5%
4	4.7K +/- 5%
5	24K +/- 5%



1. Version CX : Don't Support Mirror Code
2. Version DX/EX/FX : Support Mirror Code
3. For Mirror Code "H" --> Enable
4. "L" --> Disable (Default)

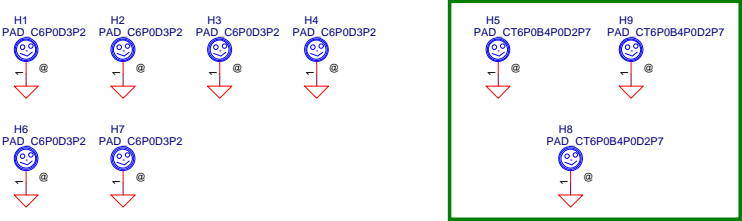
AC IN, need to confirm the pin is High or Low active while pulg ACIN



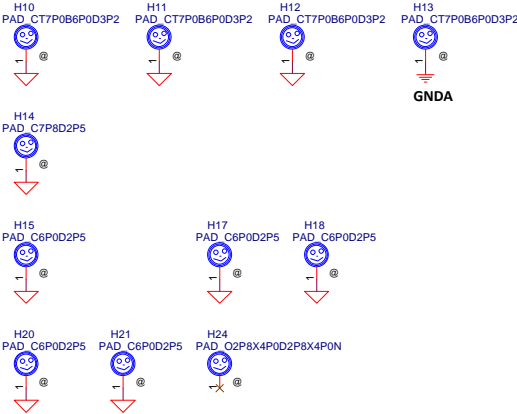
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2016/01/12		
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Screw Hole

For CPU and GPU



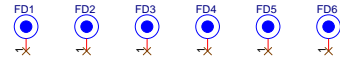
For ME GND hole




For ME hole



PCB Fedical Mark PAD



5	4	3	2	1
D				D
C				C
B				B
A				A


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				Document Number BL460_NW-A651	Rev 0.1
				Date: Friday, October 23, 2015	Sheet 79 of 99

1


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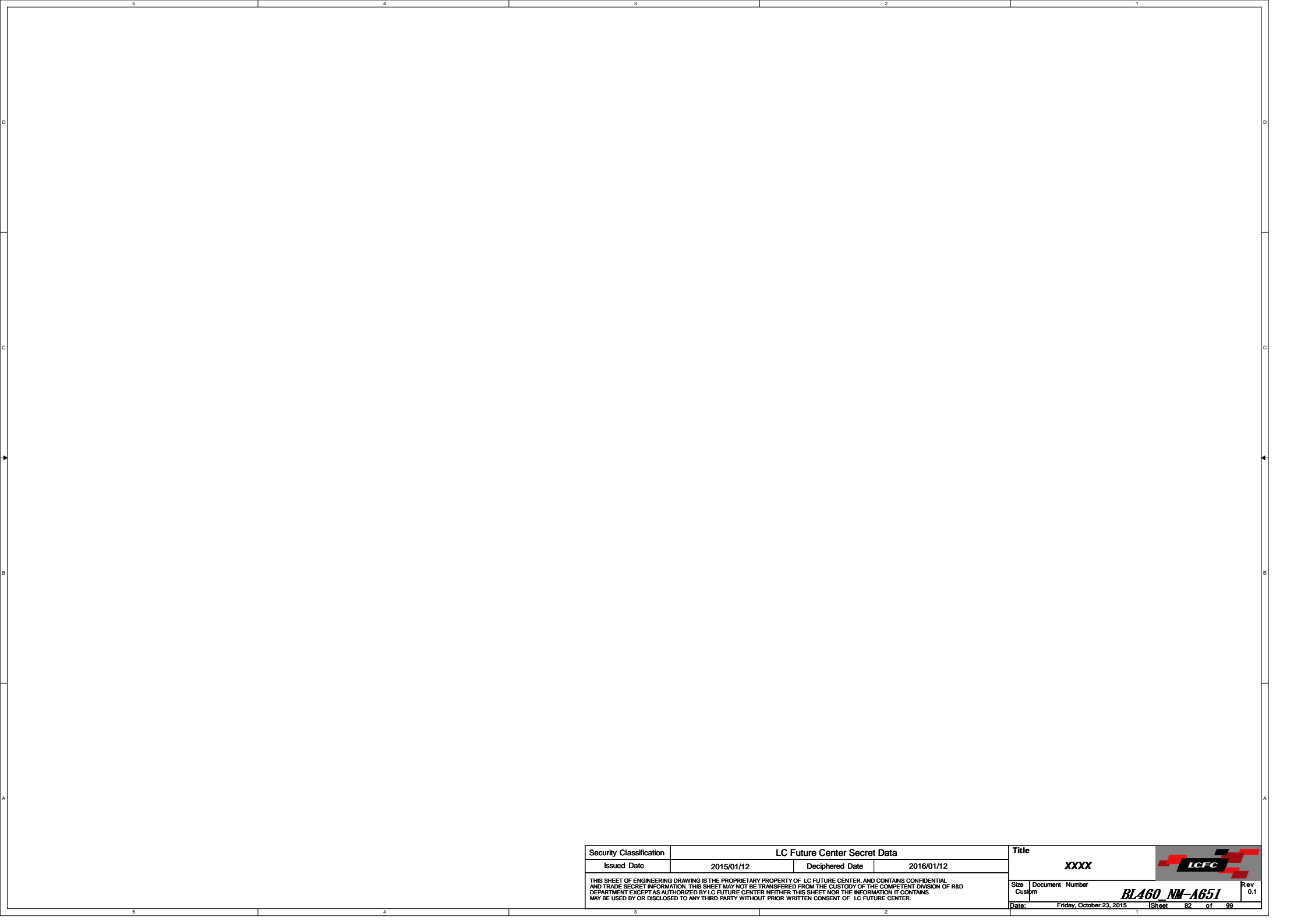
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1

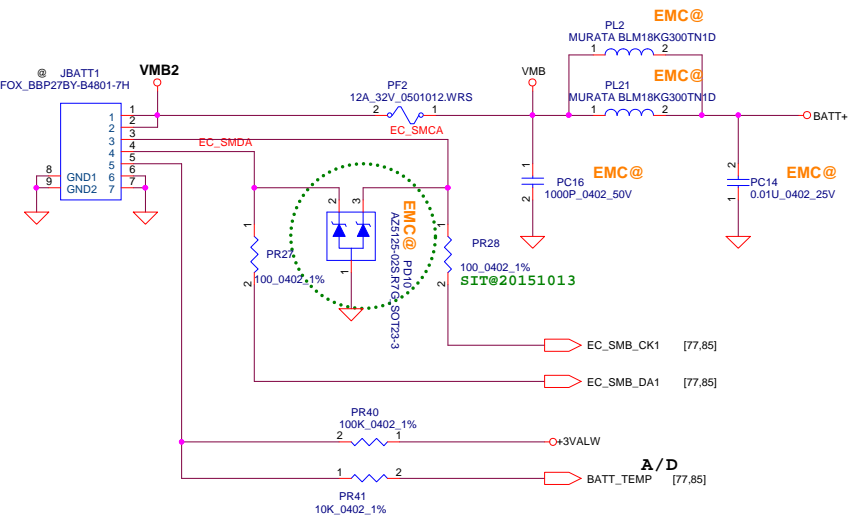
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				Date:	Friday, October 23, 2015	Sheet 80 of 99	

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D					
C					
B					
A					

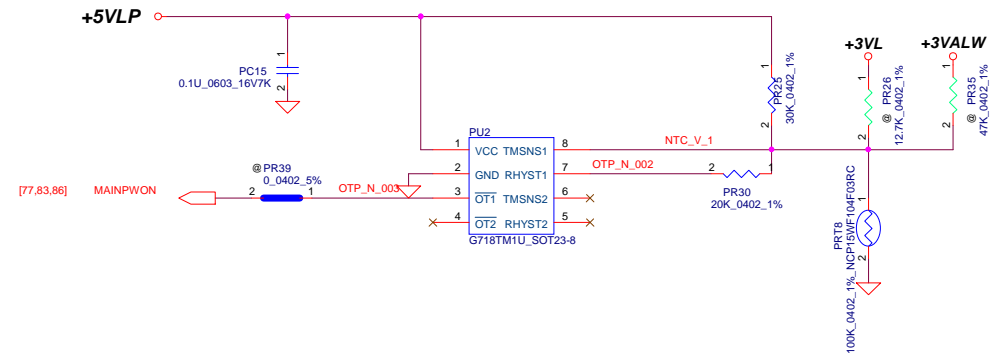
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Date:								Friday, October 23, 2015		Sheet	81	of	99

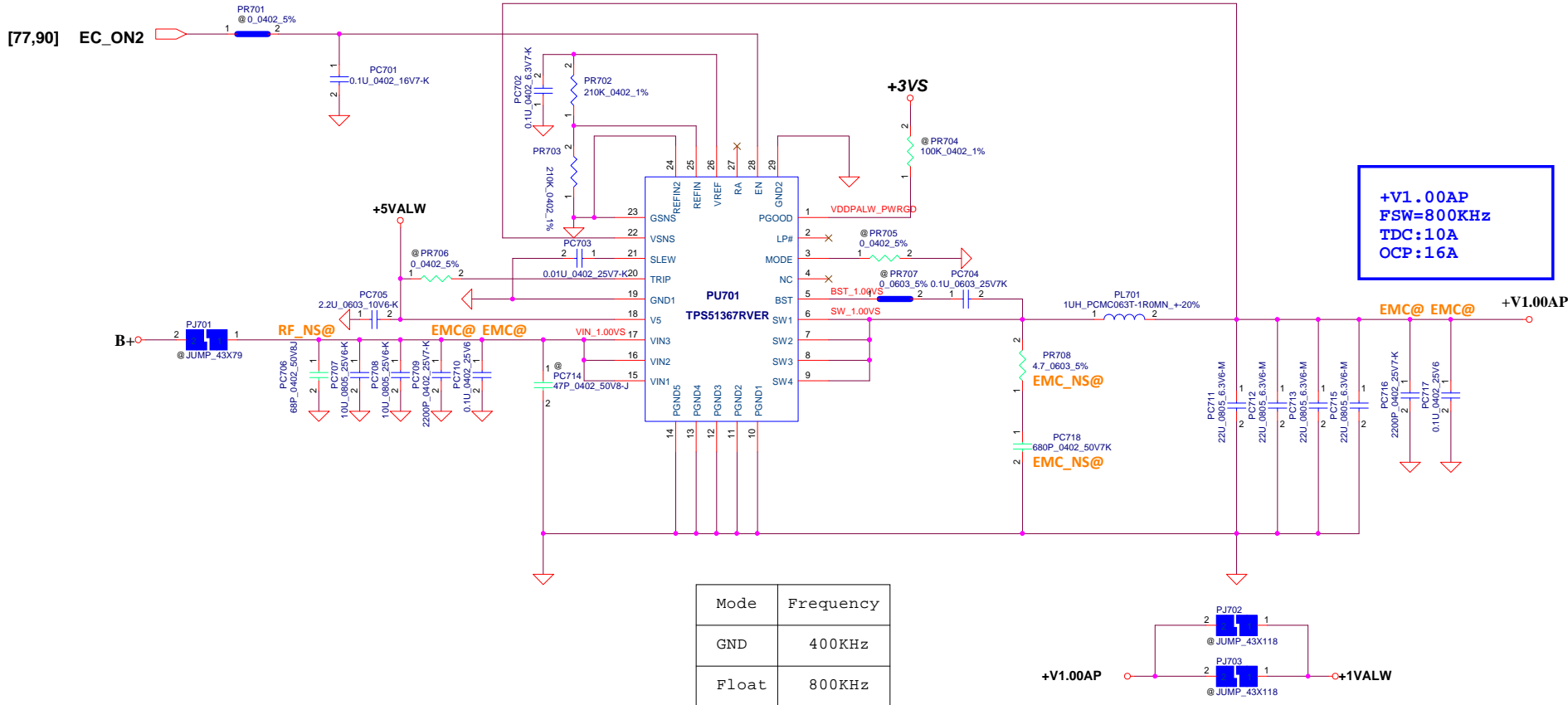



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Custom				BL460_NW-A651		0.1			
Date:		Friday, October 23, 2015				Sheet		82 of 99	

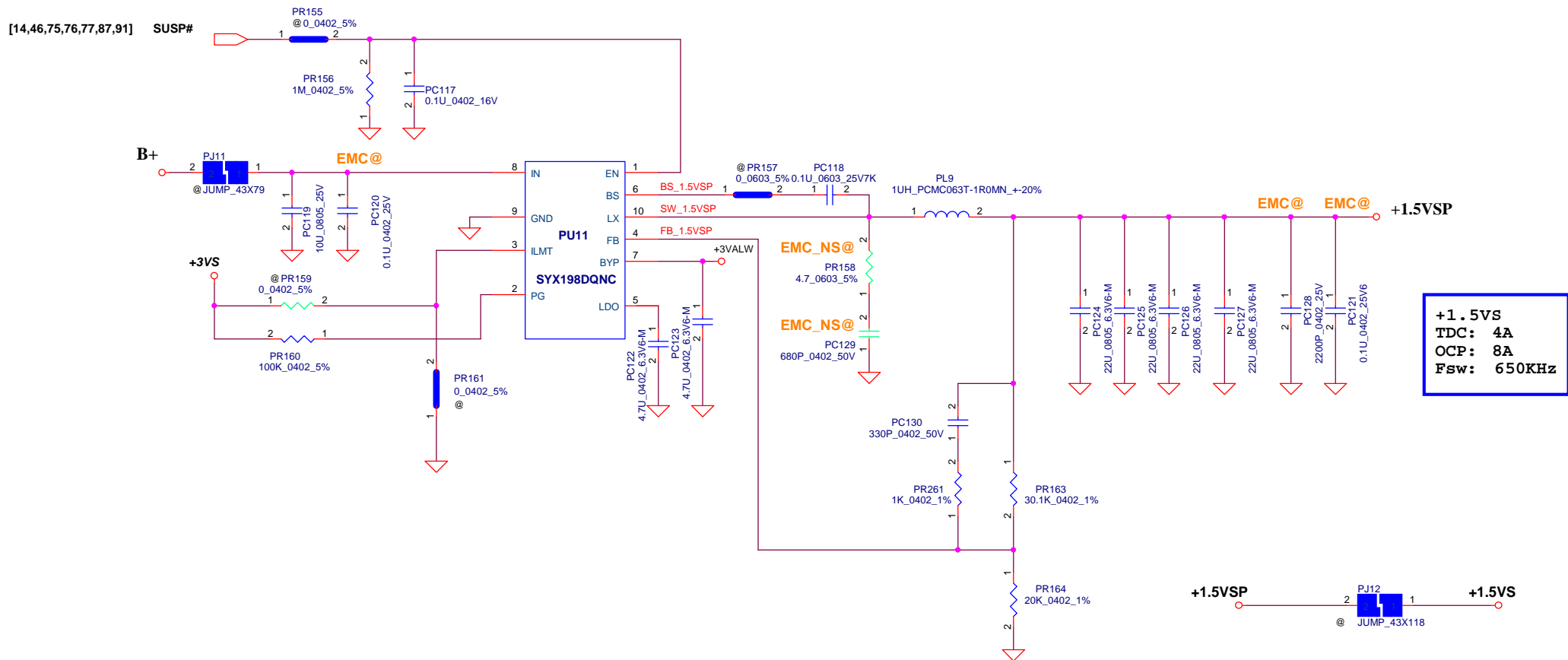



PRT8 under CPU botten side :
CPU thermal protection at 92 +-3 degree C
Recovery at 60 +-3 degree C

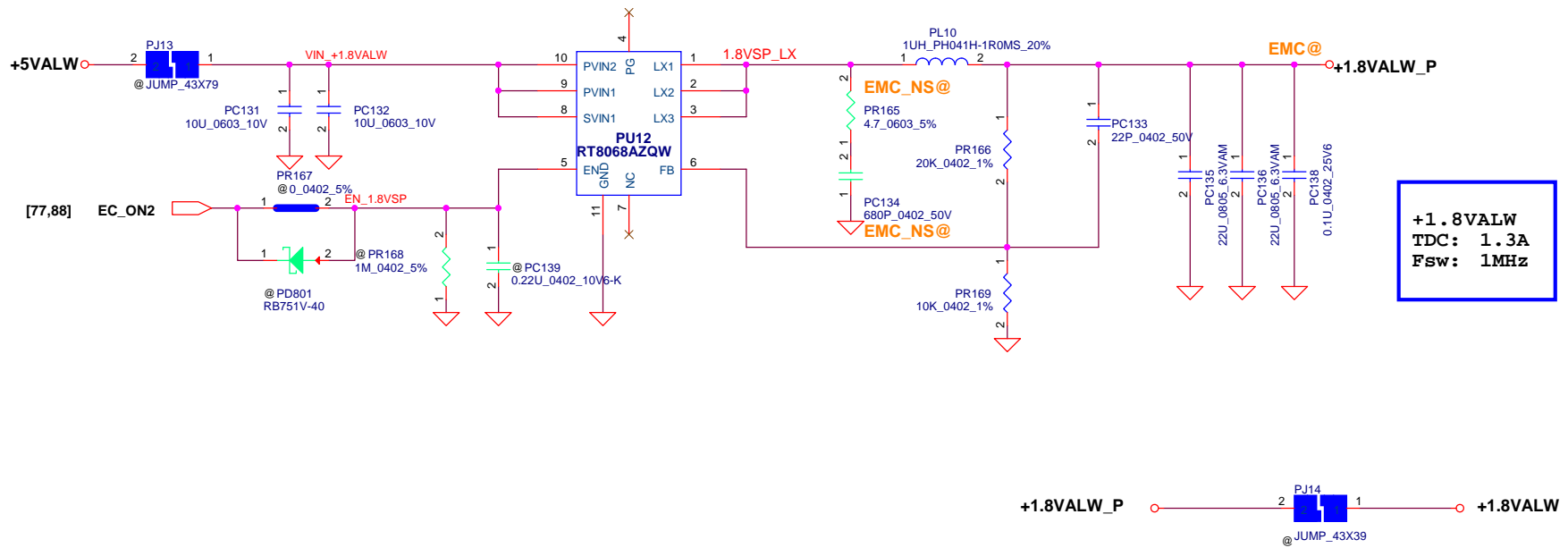





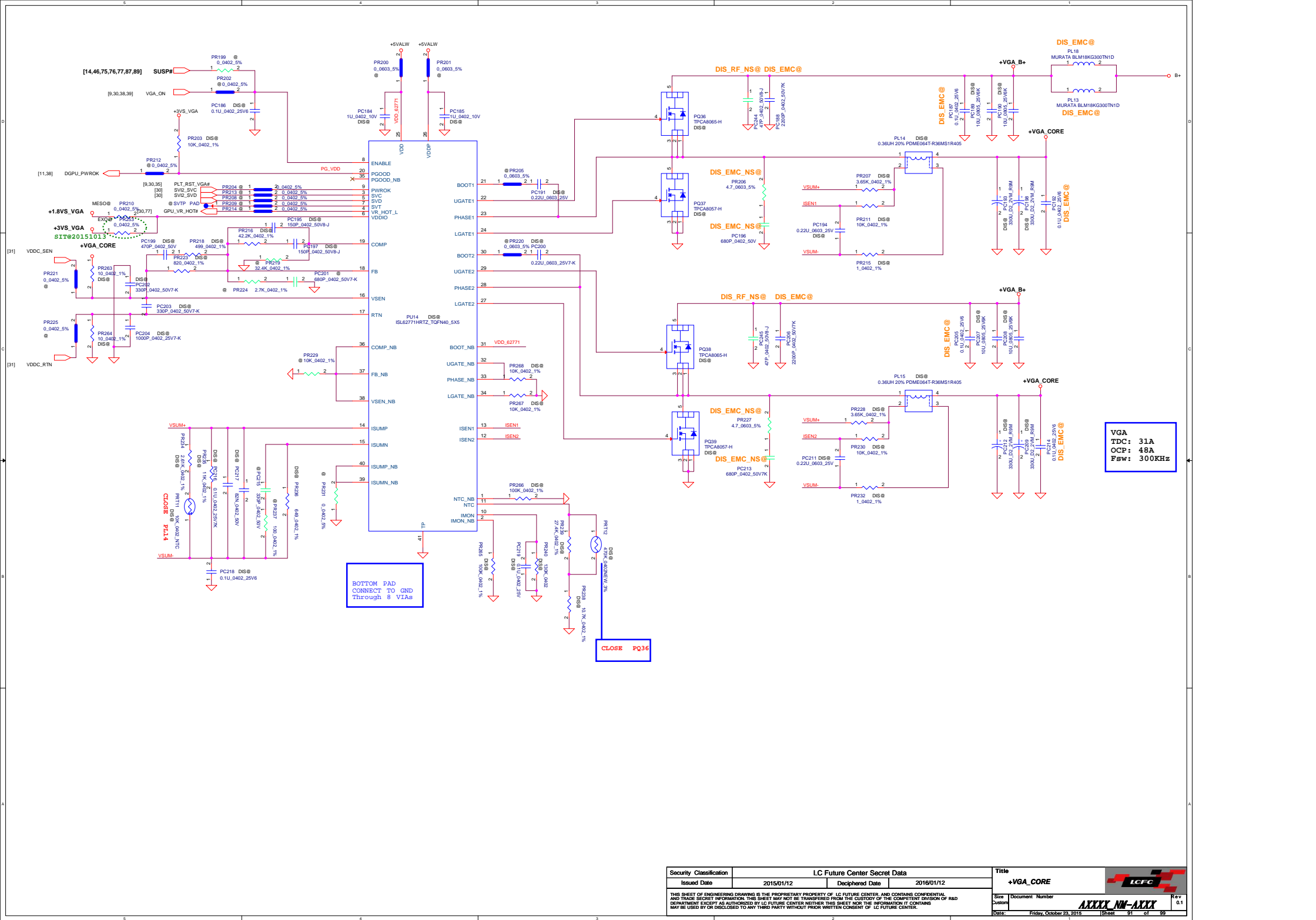
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Issued Date	2015/01/12	Deciphered Date	2016/01/12	+V1.00A		
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				Date:	Friday, October 23, 2015	Sheet 88 of 99



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Issued Date	2015/01/12	Deciphered Date	2016/01/12	+1.5VS					
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				Date:		Friday, October 23, 2015		Sheet	89 of 99

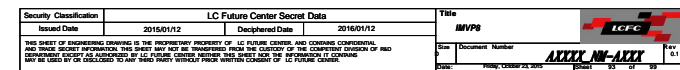


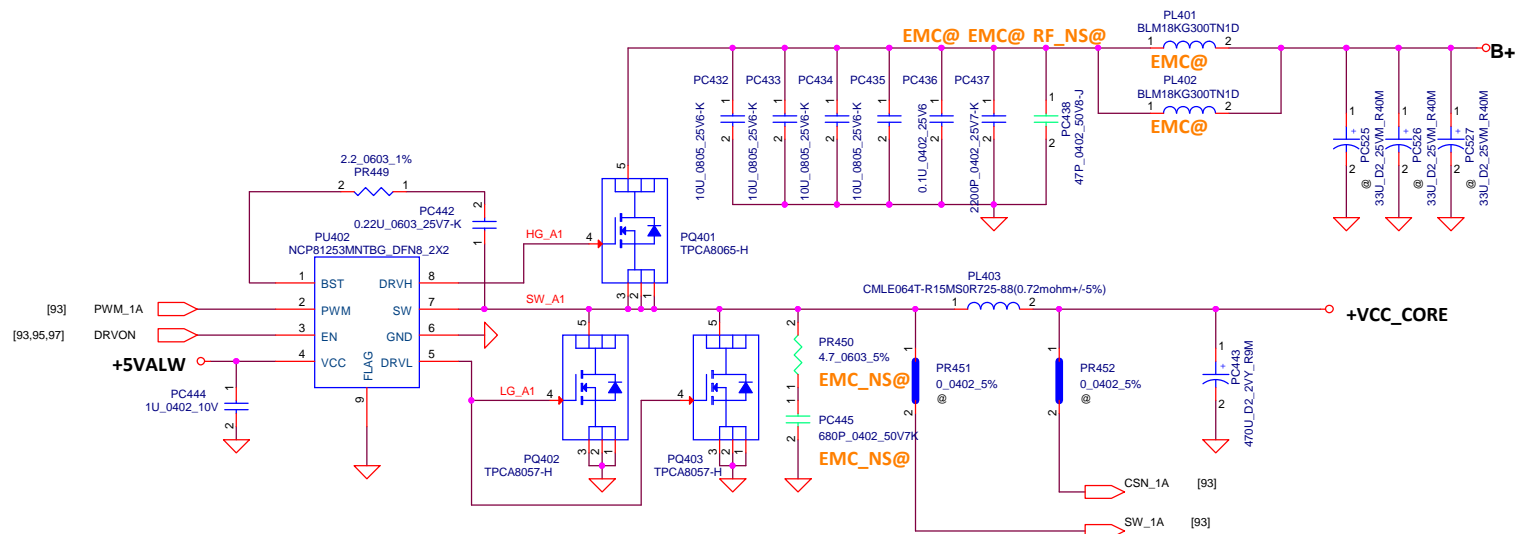
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				Date:	Friday, October 23, 2015	Sheet 90 of 99	0.1




5	4	3	2	1																													
D				D																													
C				C																													
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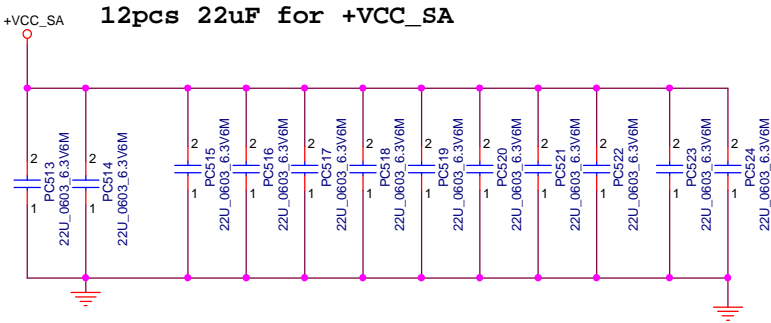
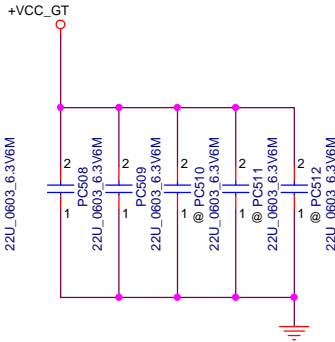
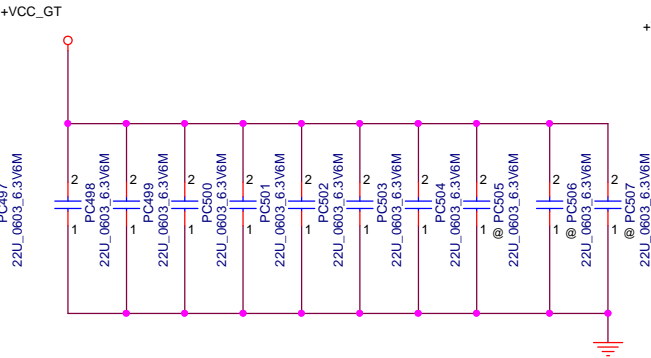
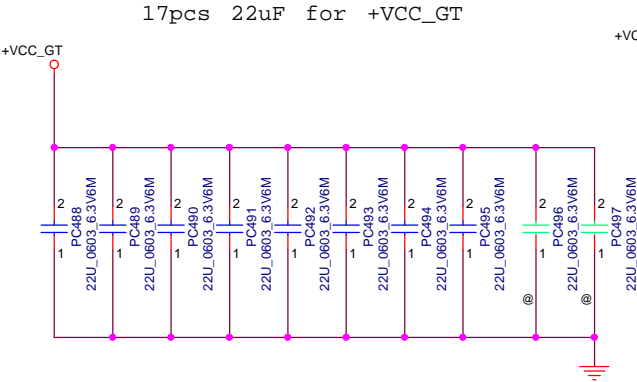
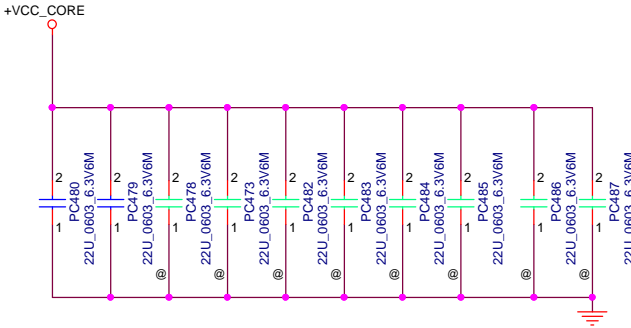
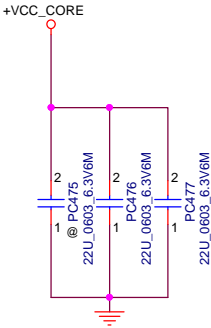
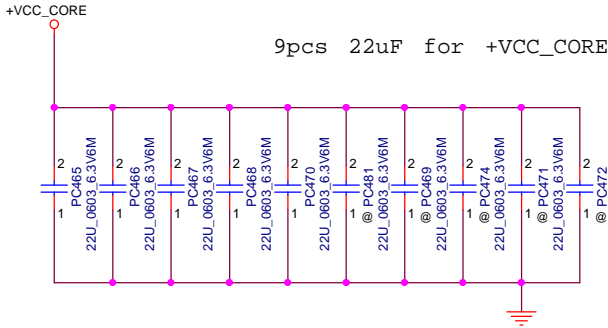






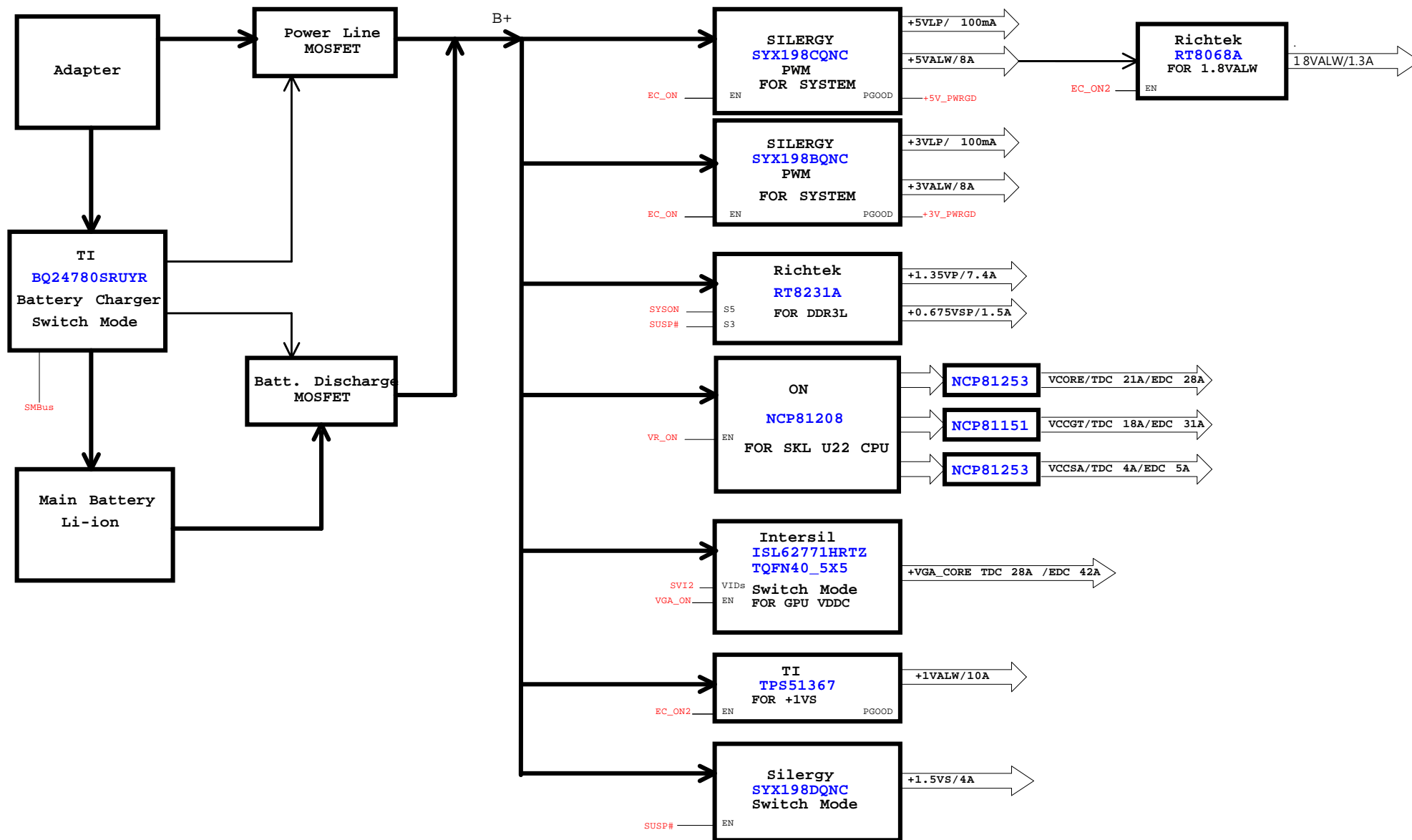
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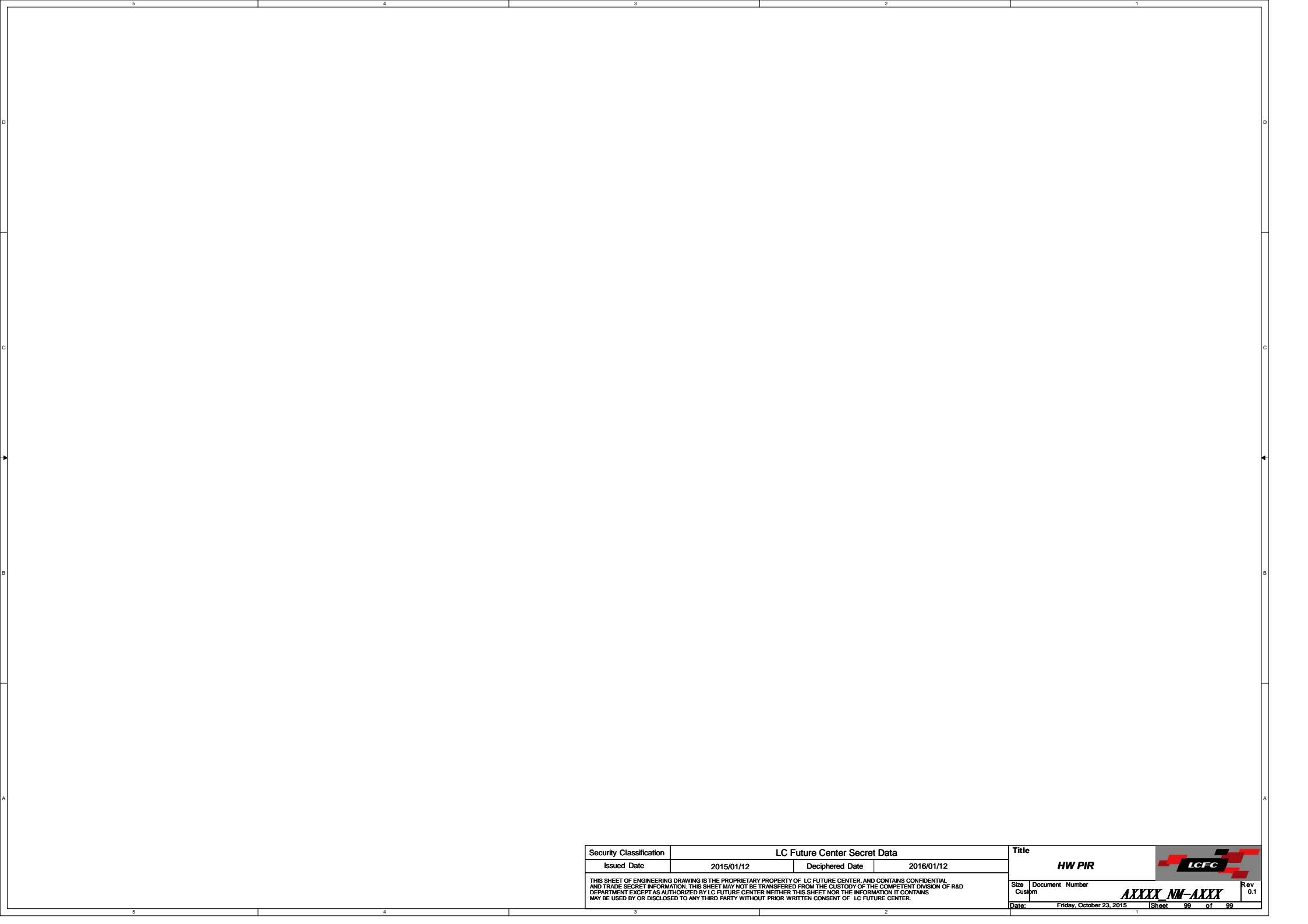
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